KEK

Development of Triggered Scaler and its Field Tests in J-PARC #1

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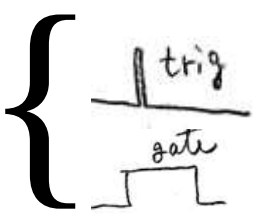
June 2018 in ANL, kami, J-PARC/KEK

Motivation

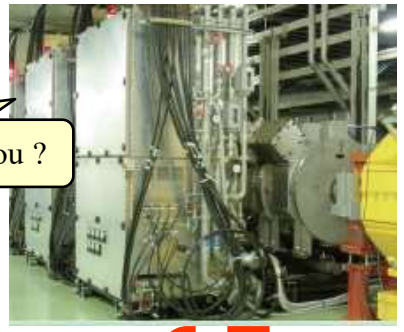
Event Timing System
(J-parc original, VME, not MRF)

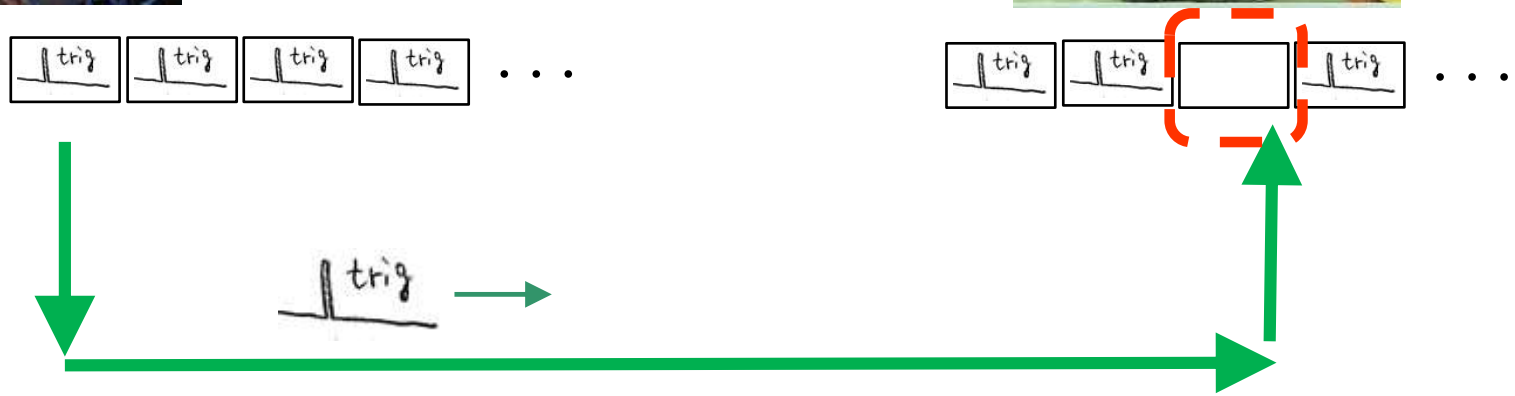
Pwr-supply, beam-diag., ..
(Photo is RF cavities in J-parc MR)



I do generate signals for you !

Ah, you missed one shot, don't you ?





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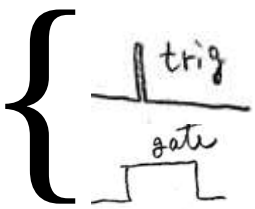

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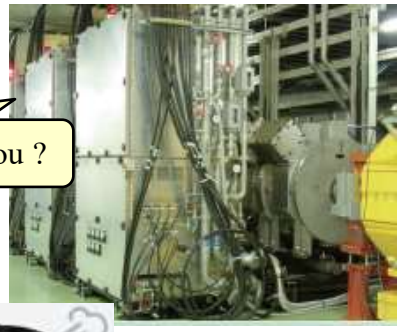
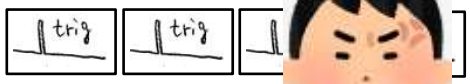


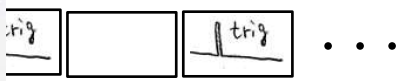


It's a fault of your side !

No, I am always perfect !

Did you check your system ?

How about you ?



To find an origin of miss-trigger is not easy ..

Typical transfer line is a fiber-optic cable: 10-50m in MR
(E/O and O/E modules exist between)

Trigger detection system

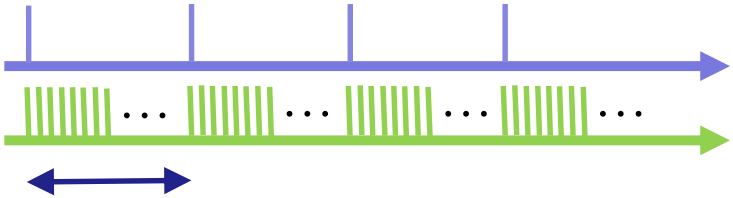
Trigger detection system

- Develop a new "trigger detection system"
designed for J-PARC accel. timing structure
25Hz (for LI,RCS) and 2.48s/5.20s (for MR, "Machine Cycle")

What is “Triggered Scaler” ?

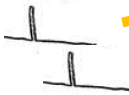
- a scaler with dual memory-buffers
- a Yokogawa PLC-type module
- Prototype in 2016, now(2018) in field test

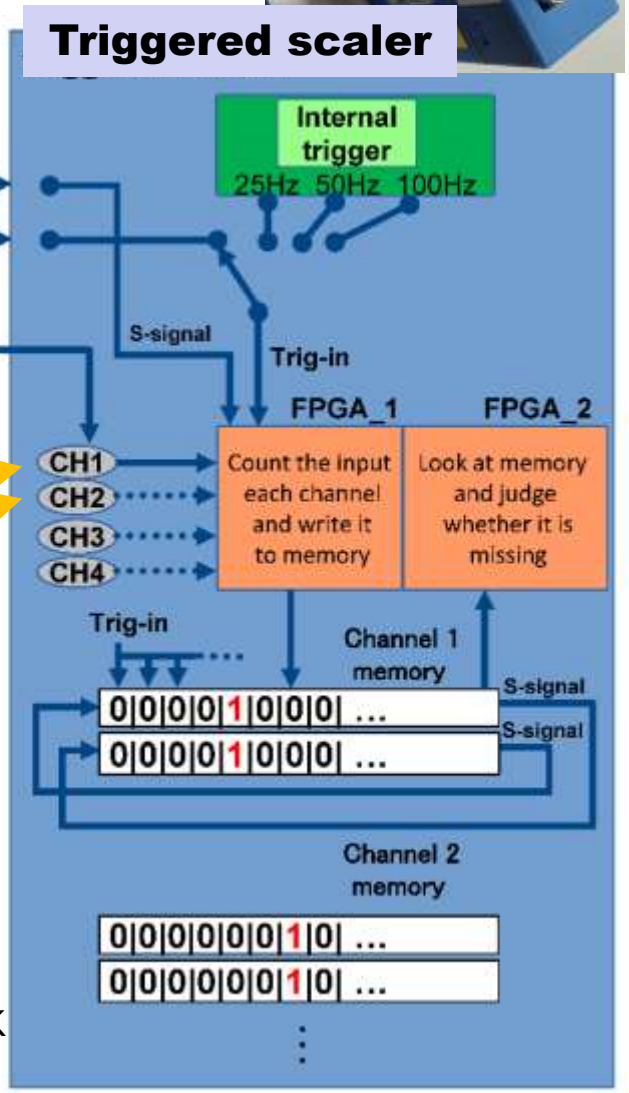
J-PARC Timing System



Machine Cycle
(2480ms or 5200ms)

Signals to be measured



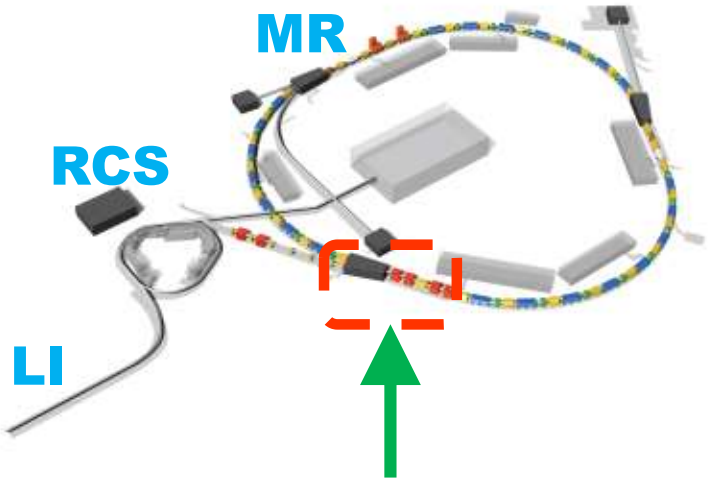


The module (FPGA_1)

- count number of pulses in 40ms-bin, store it in memory
- “Trig-in” shifts the pointer to a memory buffer
- “S-in” changes the memory buffer (+ clear pointer position)
- dual buffers, each has 192 elements (max 7680ms)

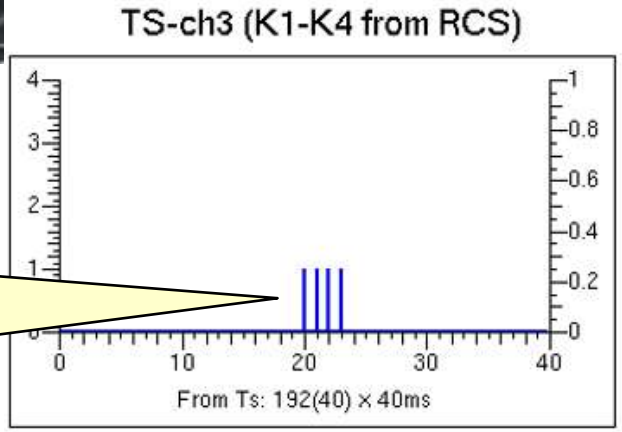
Early test in Jan. 2018

- Measure “K1-K4” triggers for the MR injection kicker system
- Four successive triggers (inject 4 time in a Machine Cycle)



Injection kicker system of MR
- Accept 4 injections (so-called K1-K4) per Machine Cycle

Trigger detection system:
- Yokogawa RP61 CPU (**Linux/EPICS**)
- a **triggered scaler module**



Observed Successfully (^o^)

Observed (CUI)

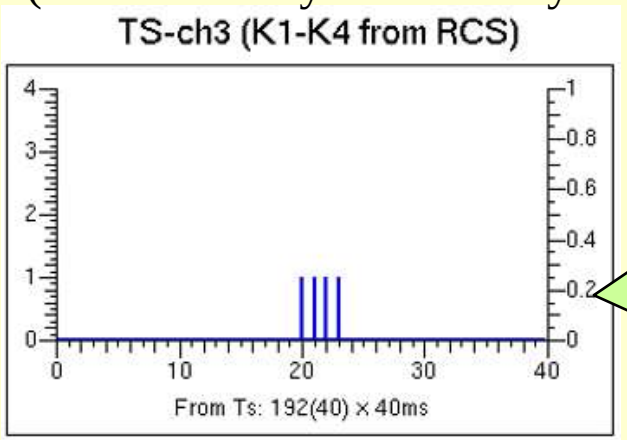
```
opr3@jkjnuc13 [173]% caget -# 138 pioc-cont-test08:TS0:WF:ch3
pioc-cont-test08:TS0:WF:ch3 138 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
opr3@jkjnuc13 [174]%
```

When a miss-trigger occurs

- How “K1-K4” triggers looks like ?

Normal

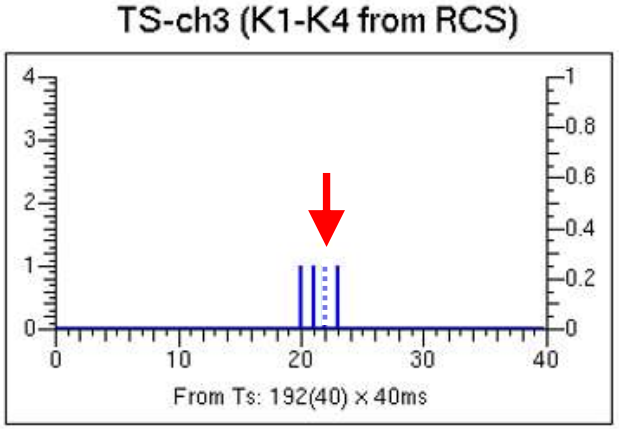
(renewed every Machine Cycle)



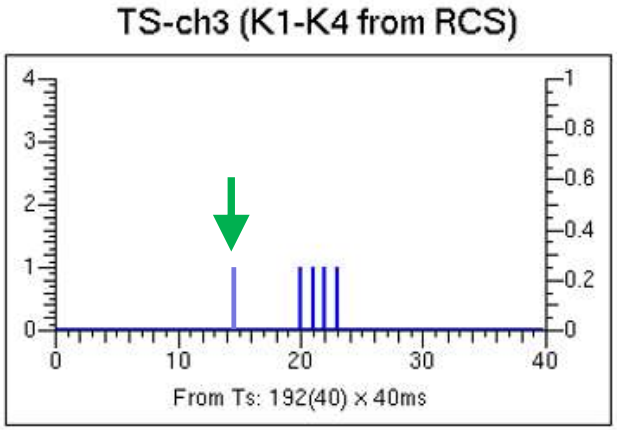
Observed

Expect

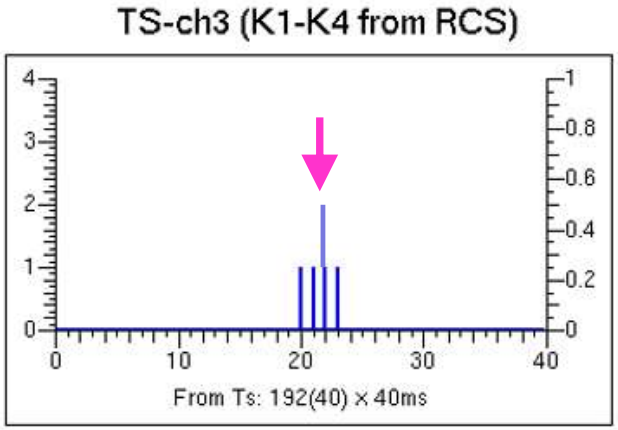
miss-trigger



irregular trigger (by noise)



double trigger (bad termination)



Plan to detect miss-triggers is in progress

Summary

- ”Triggered scaler” has been developed for J-PARC accelerator
  - as a Yokogawa plc module
  - prototype version
  - filed tests started since Jan.2018

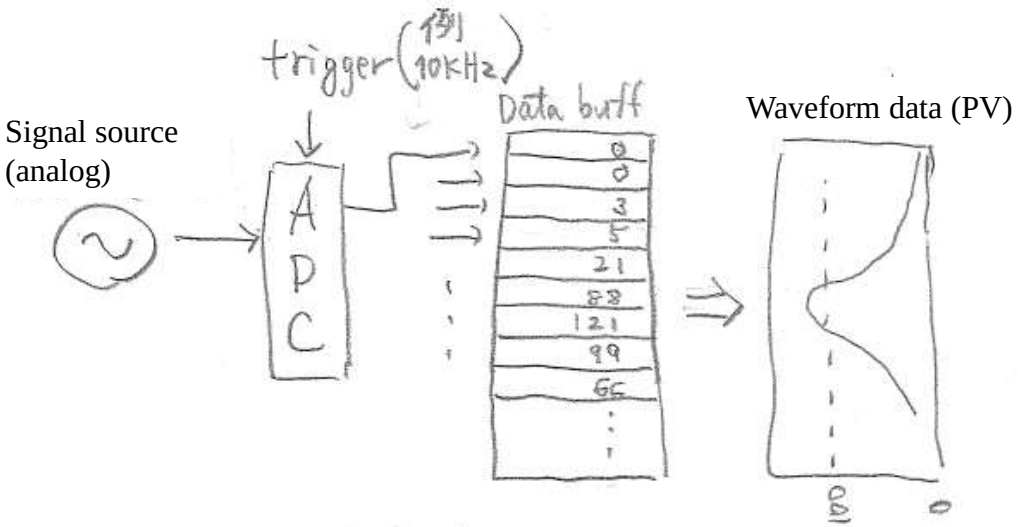
- Basic functionalities were confirmed
  - it works ! as we expected
  - plan to detect miss-trigger events is in progress

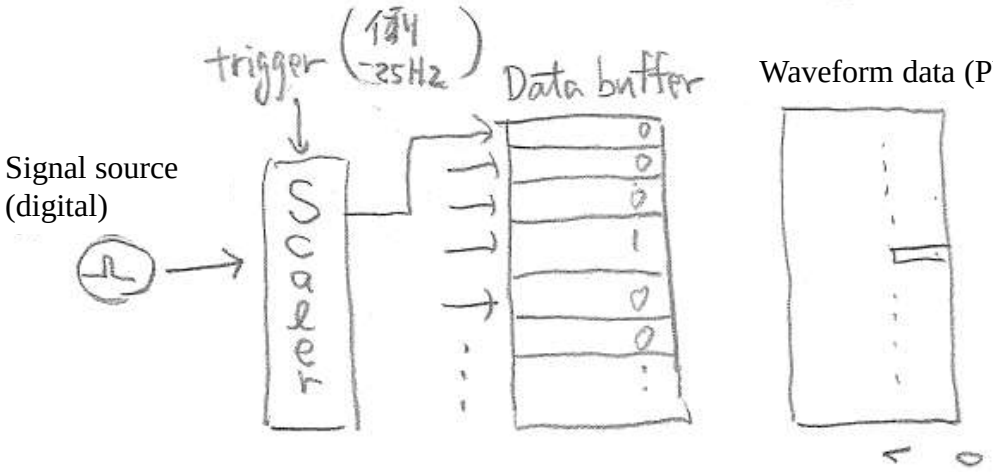
Next talk will show other demonstrations

Appendix: backup

What is Triggered Scaler （続き）

- 機能比較
  - **Digitizer (triggered ADC) and Triggered Scaler**





- Triggered Scaler for J-PARC MR:
  - default trig. rate is **25Hz** (up to 1kHz)
  - **buffer size is 192/ch**, each element 16bit
  - (not shown in the figure) **double-buffer**, switch-over is made by external S-signal (start of Machine Cycle)

J-PARC Timing: Facts in short

1. J-PARC is an accelerator complex located in Ibaraki, Japan
    1. Rapid cycle: LI(400MeV Linac) and RCS(3GeV) - 25Hz
    2. Slow cycle: MR(30GeV Main Ring) - 2.48s or 5.52s (5.20s after Jan.2018)
2. Hardware
    1. Home-design VME modules for control, NIM modules for signal generation (not MRF-based)
3. Software
    1. Developed by ourselves
    2. EPICS and its tools are used in general
    3. Java and python are preferred for table-data handling (epics waveform)
4. Scale of the system
    1. One Send-module (=EVG)
    2. LI/RCS/MR – 118/43/45 VME receiver-modules(EVR), ~540/220/300 endpoints

Base-Signal Distribution and VME/NIM Modules

Fiber-optic cable network:
- single-mode cables (3 cores used)
- 3-4 us distance between buildings

1
Send
CCB
(central control building)

~15
Recv
MR-D3
(MR 3rd build.)

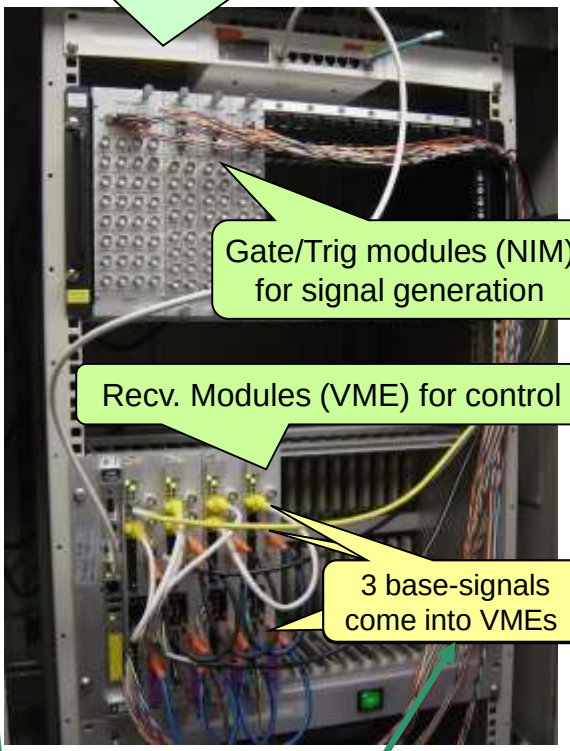
~15
Recv
MR-D2
(MR 2nd build.)

43
Recv
RCS
(RCS build.)

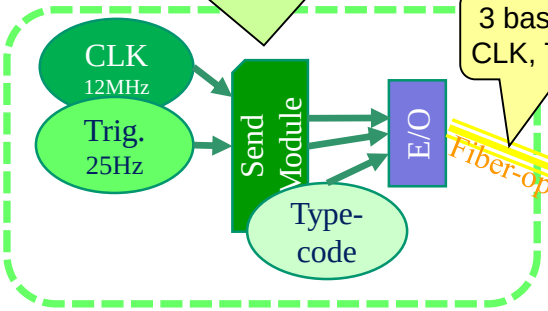
Recv
MR-D1
(MR 1st build.)
~15

118
LI
(Linac build.)
Recv

End-point example at MR-D3:
- UP : 4 NIM modules
  1 gate module (4 signals)
  3 trigger modules (8 signals each)
- DOWN : 4 VME Recv. Modules
  each module controls one NIM module



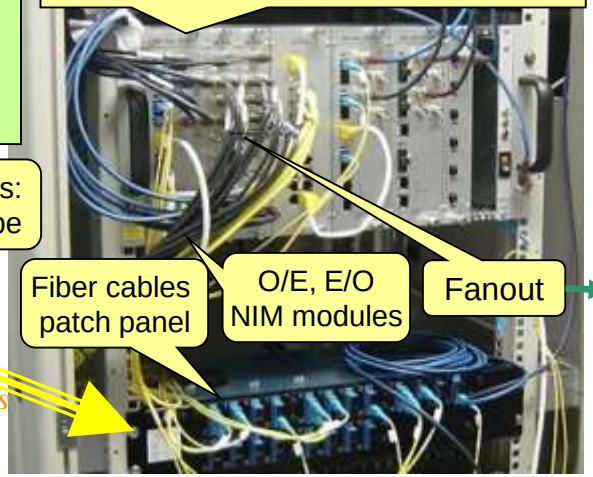
Send module located in the CCB:
- is a VME module, only one exists
- 2 Base-signals (CLK, Trig) come in
- generates series of Type-codes



3 base-signals:
CLK, Trig, Type

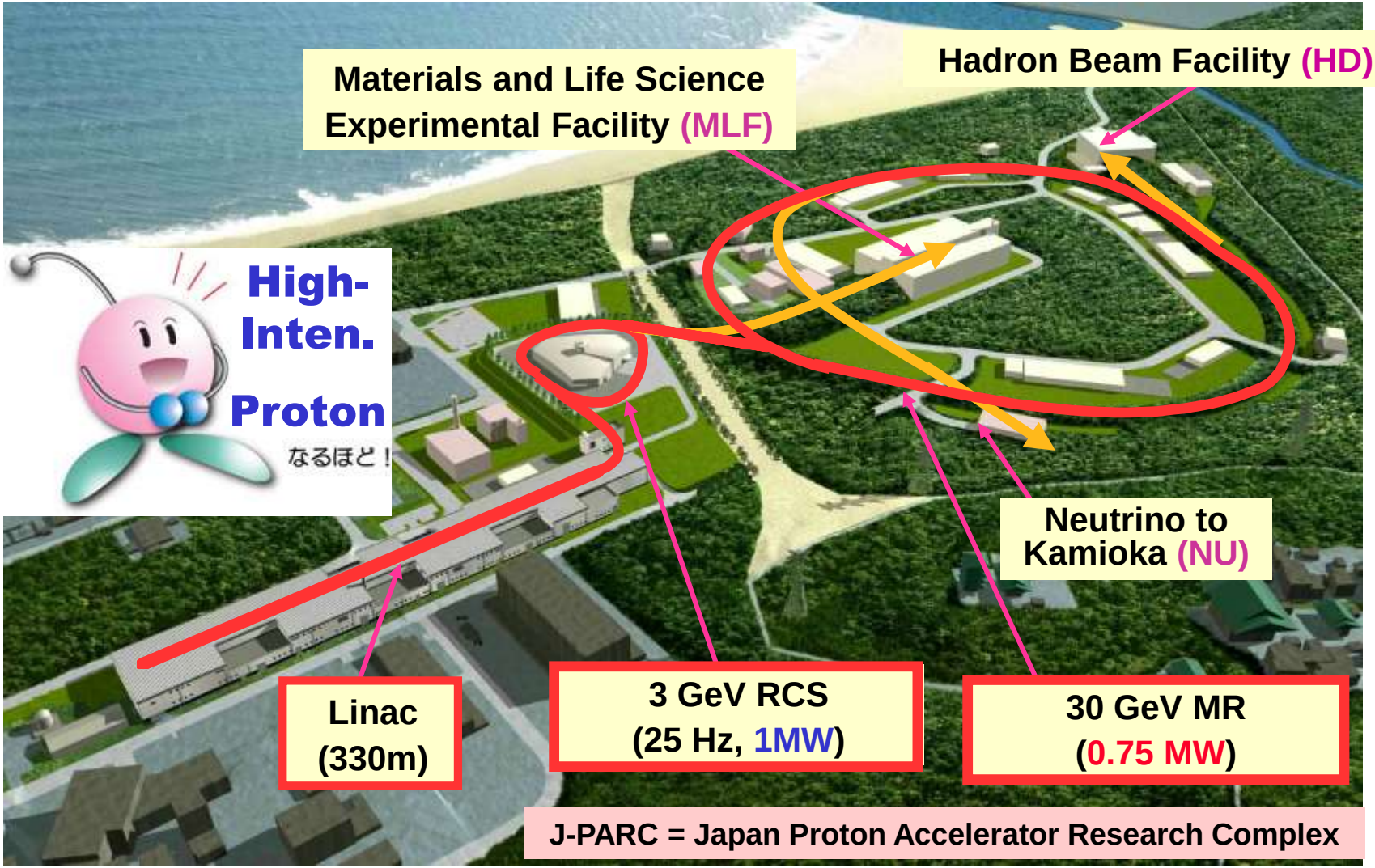
Fiber-optic cables

Base-signal distribution example:
- E/O, O/E, and fanout NIM modules

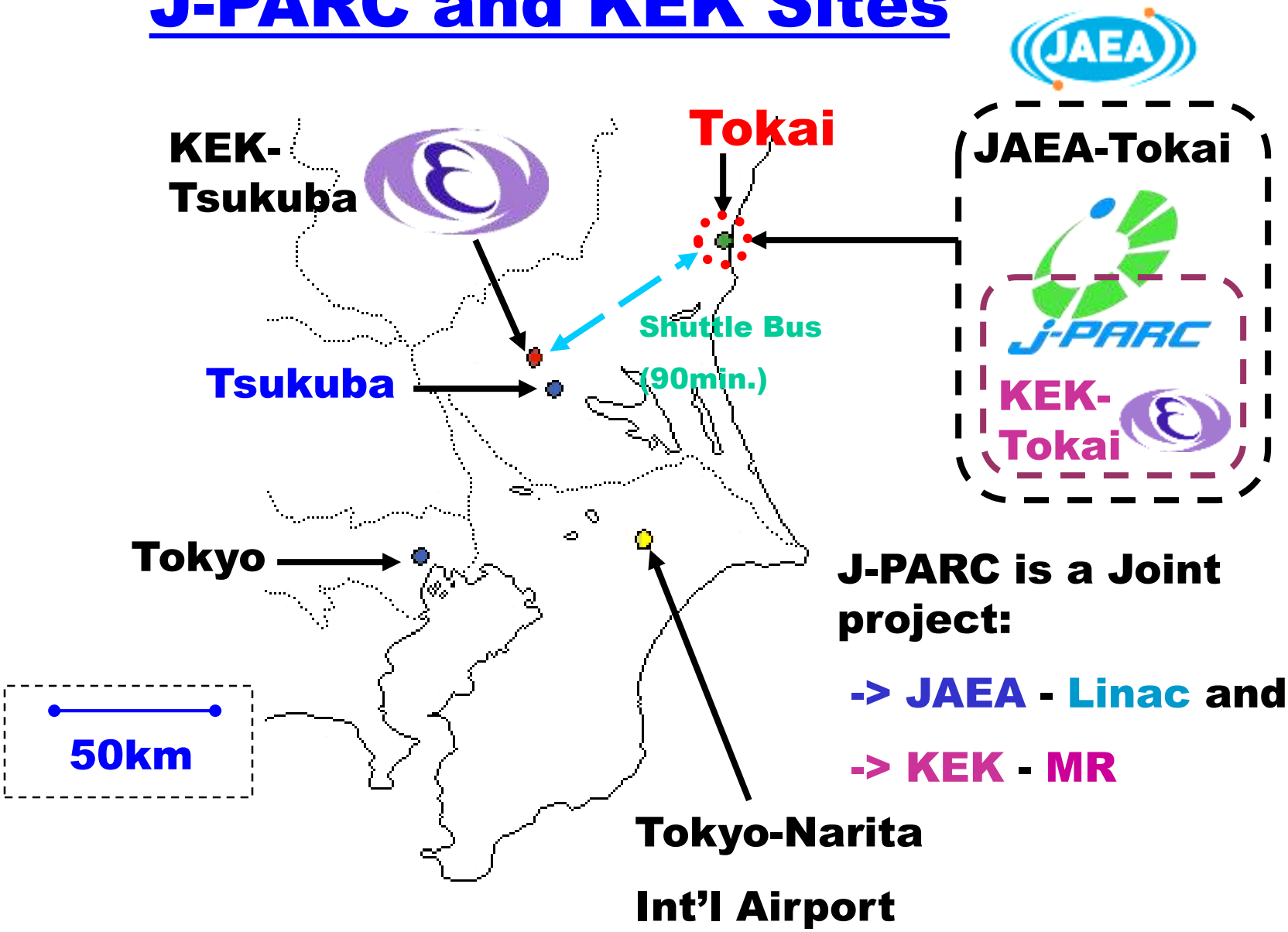


Appendix : J-PARC Facility

J-PARC Facility



J-PARC and KEK Sites



J-PARC is a Joint project:

-> JAEA - Linac and RCS

-> KEK - MR