NSLS-II new BPM status and Xilinx Zynq FPGA ARM embedded epics IOC

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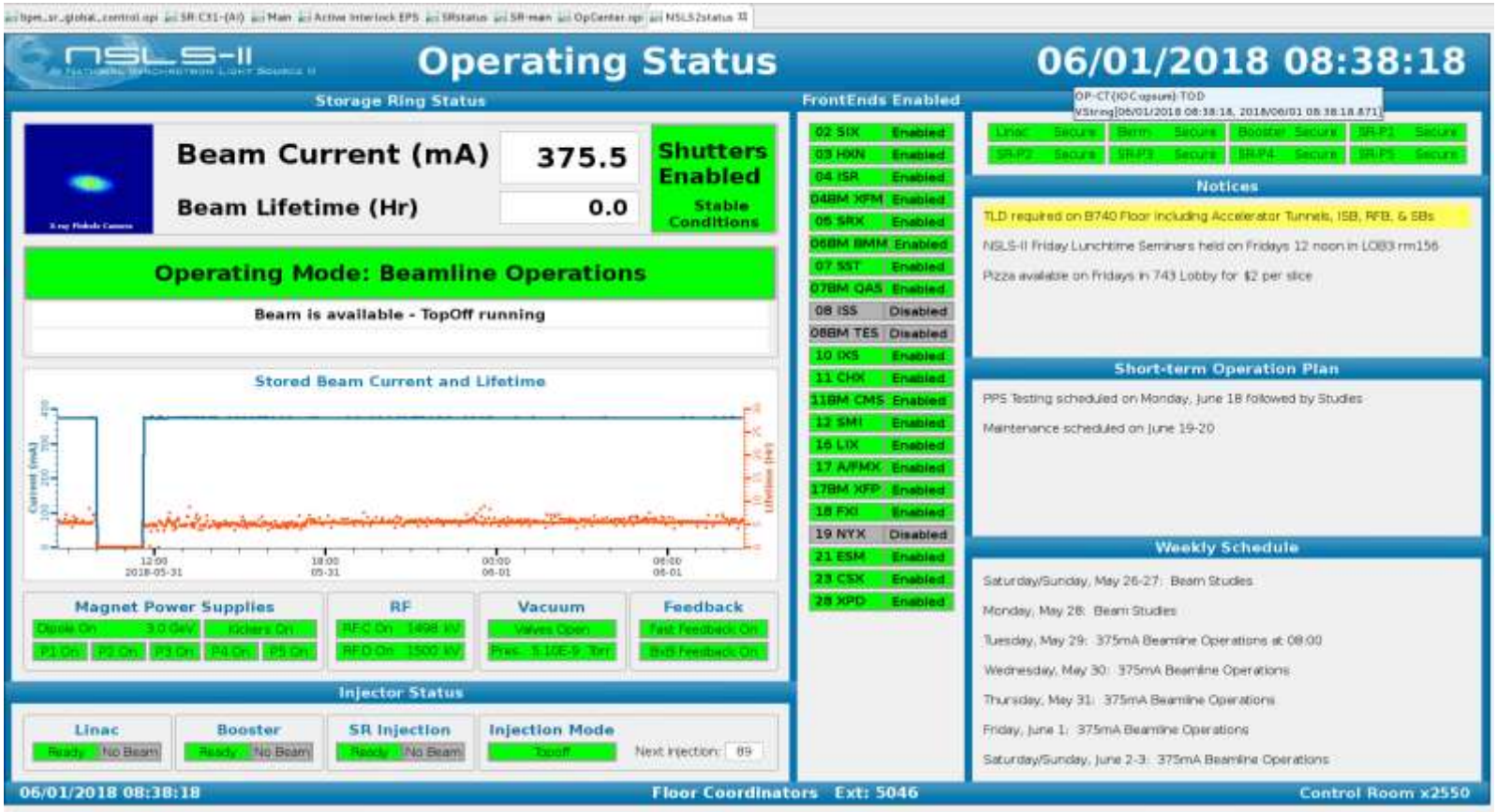
Outline

- NSLS-II Operation status
- NSLS-II RF-BPM and system configuration overview
- New zBPM overview
  - Hardware specification
  - Functional overview and beam measurement result
- Zynq embedded IOC
- Future plan
- Summary

NSLS-II Operation status

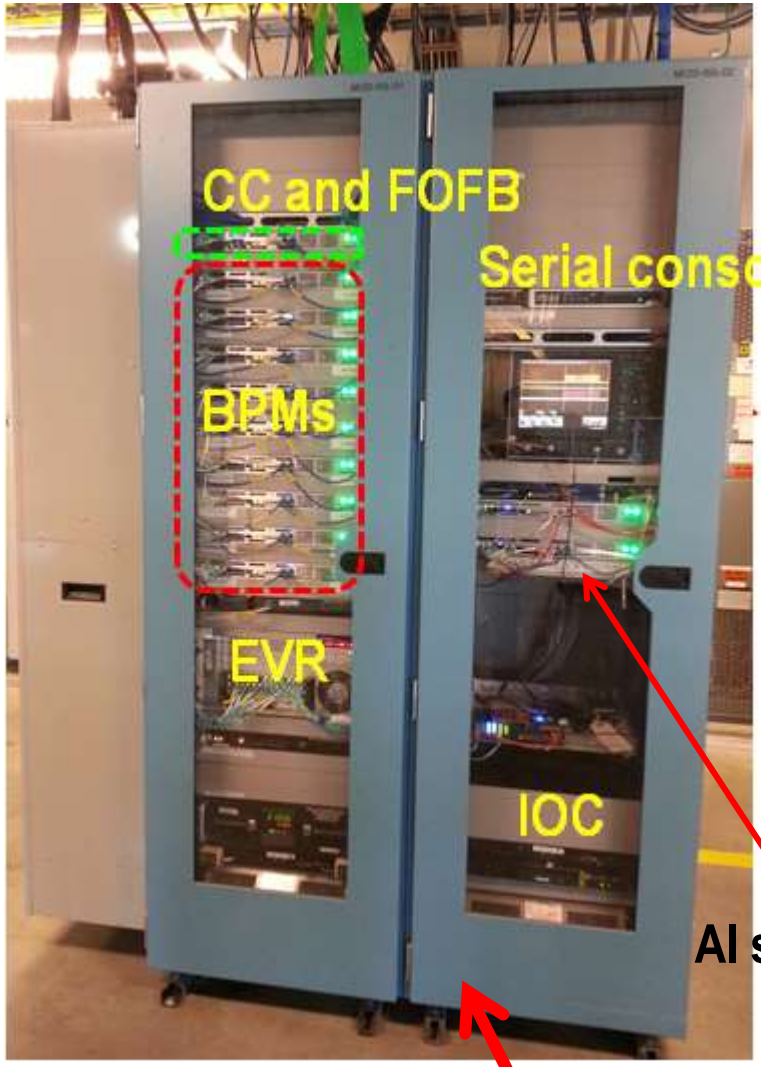


- ***Operation started Feb, 2015***
- ***Operation two super conducting RF cavity***
- ***21 Beamlines operation for user service***
- ***Beam up time in 2017 ~ 97 %***
- ***400 mA top-off injection will start this July***

NSLS-II RF-BPM

- August 2009 established BPM development team
- Fully in housed developed (2009~2013) and installed 283 units
- Design concepts:
  - Xilinx Vertex-6 FPGA device
  - Compact and modern technology RF receiver board
  - Same DFE board designed for the Cell controller and AI system
  - DFT algorithm for beam signal processing (The new firmware support DFT, CIC and FIR for 10 kHz)
  - A model-based design used System generator toolbox
  - Employed an Embedded EVR
  - Bidirectional 5 Gbps GTX data communication for the FOFB and fast machine protection(AI)
- Support two(2) Gate signal processing function(Beam processing and user interested bunch processing or online lattice characterization)
- Multiple sinewave driving for accelerator system fast response/bandwidth measurement
  - 0 – 2 kHz sinewave driving throw the local and global SDI links
- Post Mortem (ADC sum, TBT:x,y,sum, FA:x,y,sum)
- TBT Glitch detection
- Remote firmware upgrade
- Other operation related functions

RF BPM Rack and CSS main screen for operation



AI system(Fast MPS)

- ❑ BPM install status (~283)
  - Linac – 6
  - LTB – 5
  - BR - 36
  - BTS - 9
  - SR – 223 (arc 180, ID 43) Injection(4)

- ❑ 0.1 Degree C temperature controlled rack

Why we need new development

- Not system performance issue, satisfied all the requirements, performance for beam Ops
  - Contributed a lot of valuable publications based on NSLS-II BPM (Physics review, NIM, many other conferences)
  - Support two gate mode (beam operation and online lattice measurement)
  - Support PM, glitch detection (diagnostics propose)
  - Multiple sin/cos waveform driver for fast/slow corrector excitation (AC LOCO and BBA)
- The NSLS2 machine is stable and keeps continued going development work
- Already nine(9) years from the development to operation
- Virtex-6 FPGA was obsolete a few years ago
- Xilinx released advanced FPGA model (Zynq, Kintex, Vertax Ultrascale+pulse)
- Expended a new application (BxB BPM, BxB feedback, Cell controller, AI and beamline applications)
- Implement new algorithms for improving performance
  - Multi gate signal processing function
  - Digital signal processing (DFT, DDC)
  - Single bunch multi harmonic processing for improve resolution

Motivation for BPM upgrade to zBPM

- **Existing RF BPM DFE**
  - The soft-core MicroBlaze processor has limited performance and poor network performance.
  - Xilkernel OS is a non-standard, Xilinx specific, bare-metal operating system with limited support.
  - LwIP TCP/IP light version
  - Software development requires special knowledge of Xilkernel OS features

- **zDFE Improvements**
  - Hard dual-core ARM A9 processor
  - provides >500 Mbit/sec throughput
  - Runs standard Debian based Linux Operating System
  - Embedded IOC or standalone apps
  - Software development is now user space applications similar to software development on a standard Linux environment.
  - Better solutions for long term maintainability and software development
  - Allow developers easier access to maintain and upgrade software and features.
  - Provides more an FPGA resources and excellent development tools (VIVAOD)

zBPM prototype

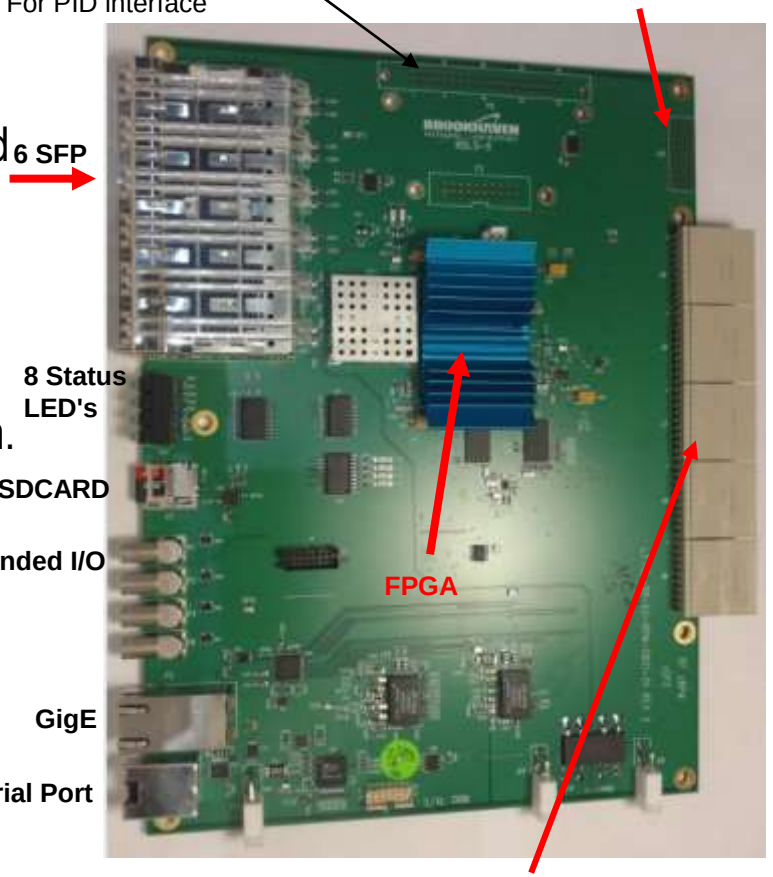
- Specs:
  - ✓ 1 U size Chassis
  - ✓ 500 nm turn-by-turn (TBT)
  - ✓ 100 nm in 10 kHz (FA)
  - ✓ 200nm Long Term Stability /8hrs in 10Hz (SA)
- Verified with beam
  - TbT used for injection & kicked beam studies
  - FA for fast orbit feedback & interlocks
  - SA for orbit measurements, System Health

Data Type	Mode	Max Length
ADC Data	On-demand	100Mbytes or 12M samples raw ADC per channel simultaneously
TBT	On-demand	100Mbytes or 2M samples TbT (Frev=378KHz) A,B,C,D,S,X,Y
FOFB 10KHz	Streaming via SDI Link and On-demand	100Mbytes or 2M samples FA (10KHz)Streaming - X,Y,SUM ; On-Demand: A,B,C,D,S,X,Y
Slow Acquisition 10Hz	Streaming and On-demand	buffer SA (10Hz)
System Health	Streaming	AFE temp, DFE temp, FPGA Die temp, PLL lock status, SDI Link status

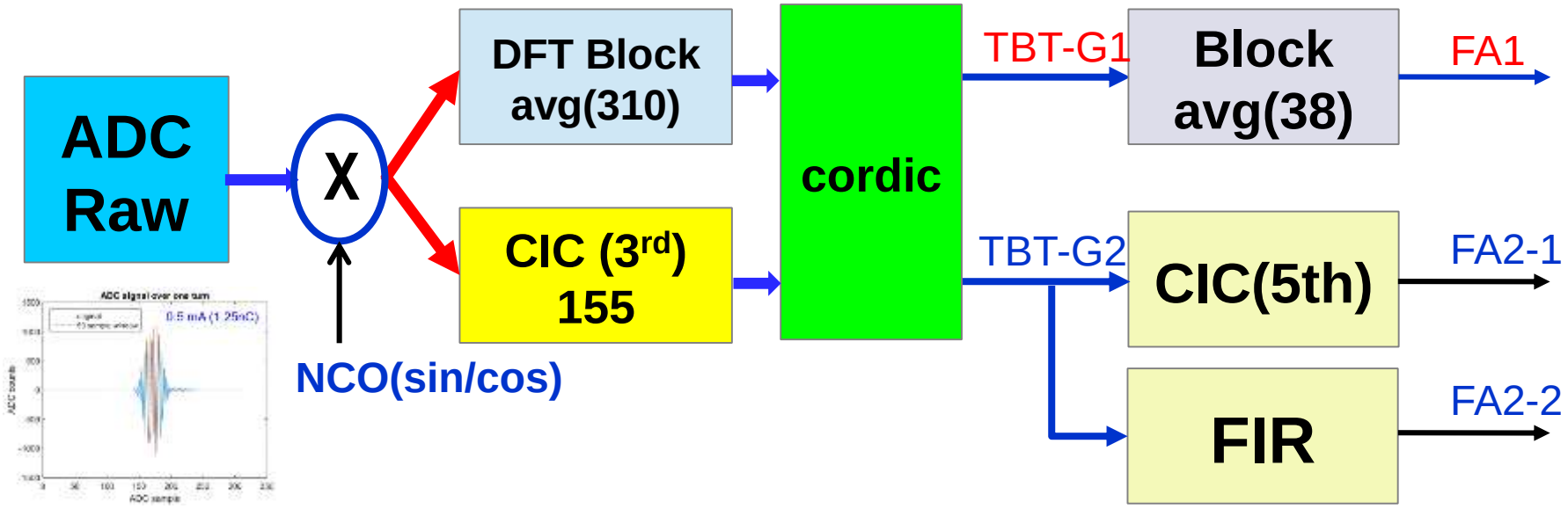
Zynq DFE board

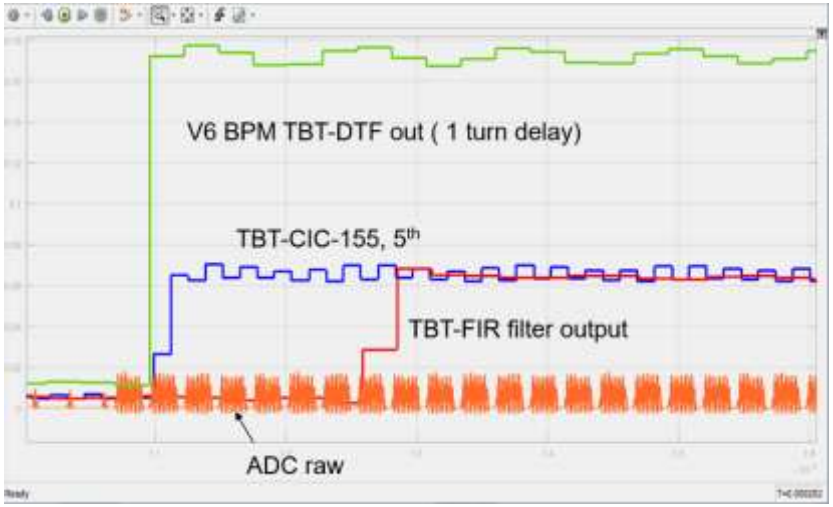
❑ Features/Benefits:

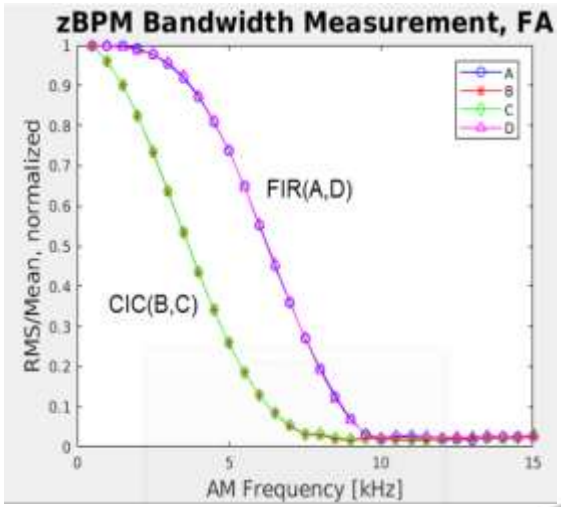
- Powerful ARM base processing
  PL: Programmable logic, PS: Processing system
- Hardware is backward compatible, use existing AFE and enclosure to minimize upgrade effort and cost
- NSLS2 standard to common DFE platform, supporting multiple sub-systems including: RFBPM, BbB-BPM, X-Ray BPM, Cell Controller for Fast Orbit Feed-Back
- Runs standard Debian-7 based Linux Operating System.
- 8 ports 10 Gbps GTX, 6 ports 10 Gbps SFP



FPGA firmware signal processing and filter response



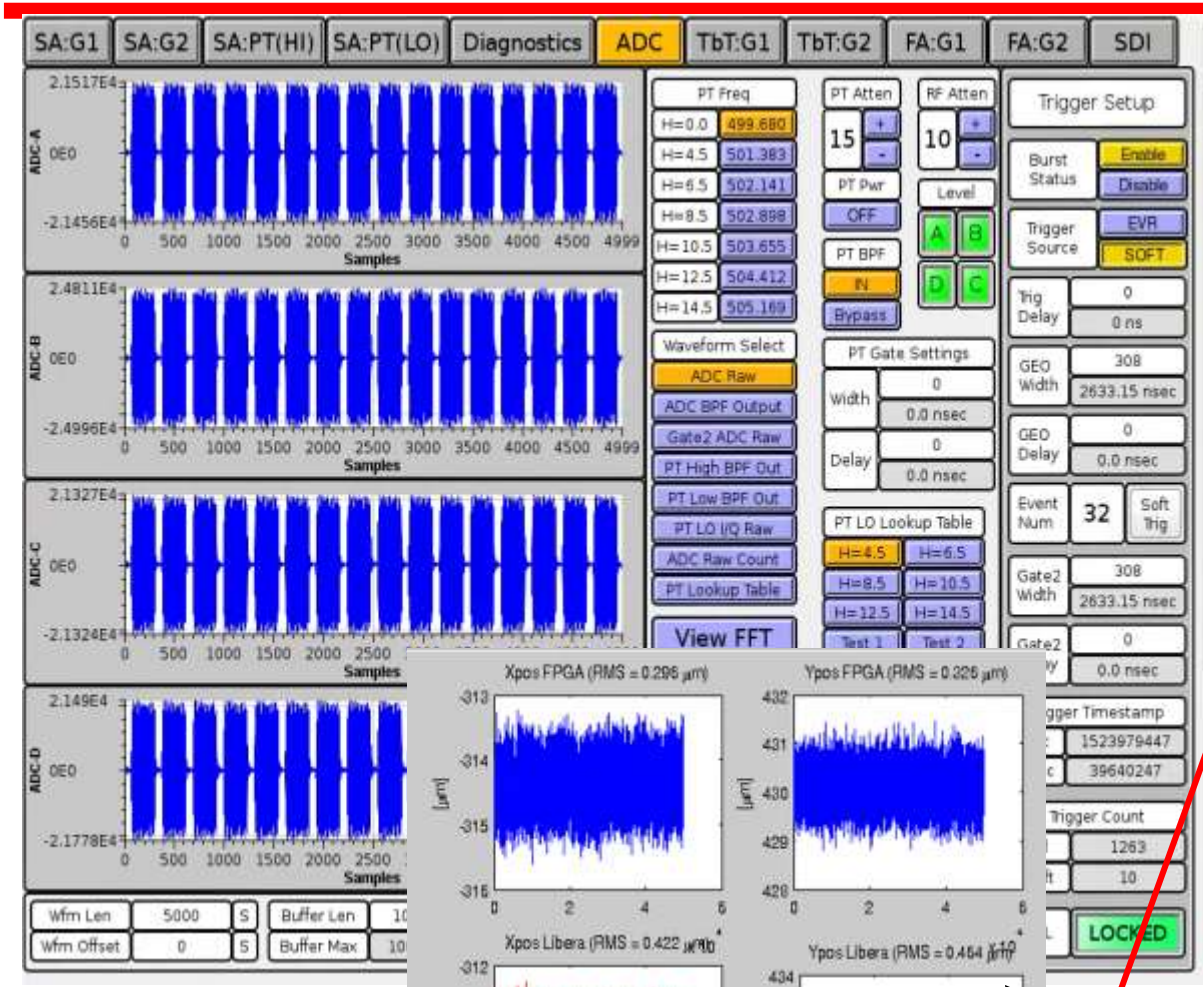


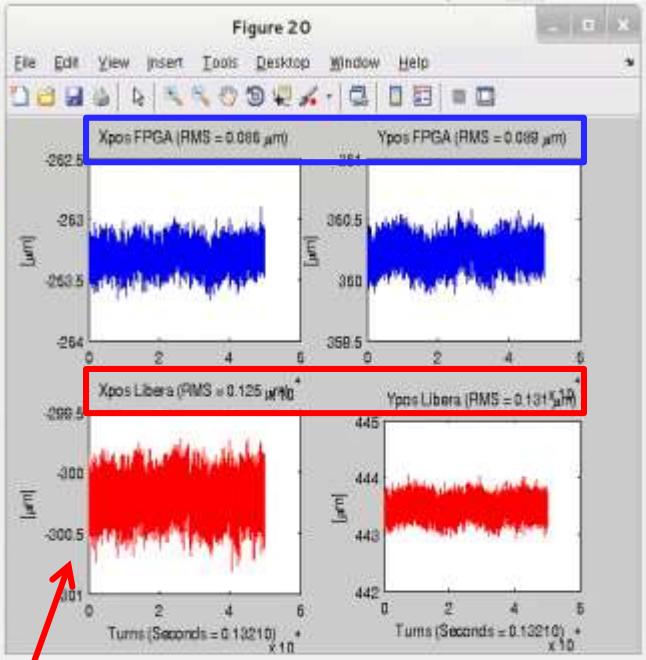


What's new for ZYNQ IOC

- Dual ARM Cotex-9 core 666 MHz
- Debian-7 ARM Linux
- Base 3.15.5
- Booting from 32 Gbyte micro SD-Card
- DMA Kernel driver for the large waveform access
  - Up to 300 Mbyte
- Not used special custom driver/record support
- aSub array record for waveform collection
- Standard epics soft recodes
  - WAVEFORM, AI, AO, BI, BO, LONGIN, LONGOUT, MBBI, MBBO
- Control system network bandwidth ~ 60 Mbyte measurement with NSLS2 gateway box

CSS top panel and Beam measurement (attenuator 10 dB)





❑ **FA(10 kHz) RMS**

DDC : 86 nm, 89 nm

DFT : 125 nm, 132 nm

****DDC is ~30 % improvement**

❑ Beam 375 mA

❑ FA

❑ TBT

❑ **Turn by turn (RMS)**

DDC : 296 nm, 326 nm

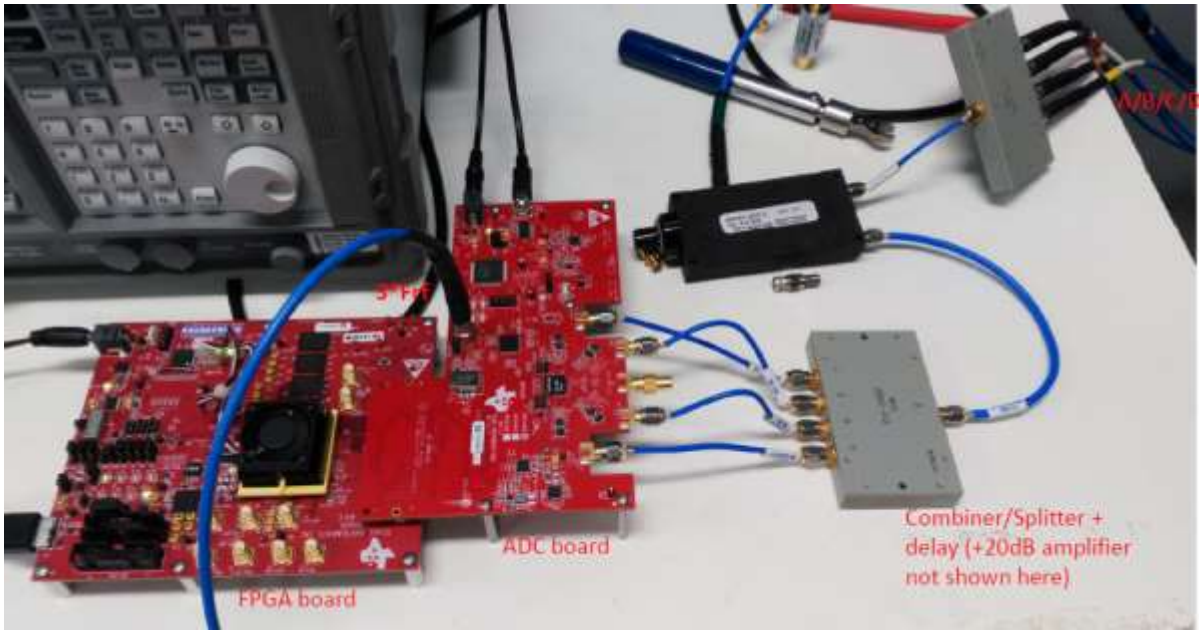
DFT : 422 nm, 464 nm

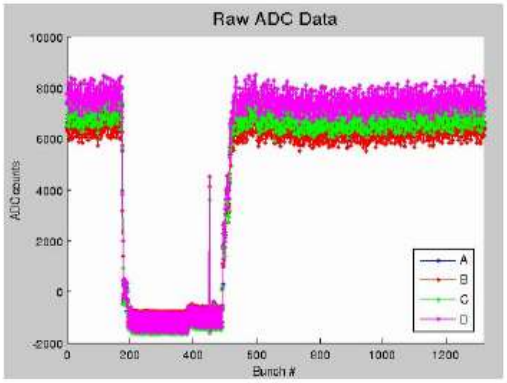
Embedded small scale IOC for Operation

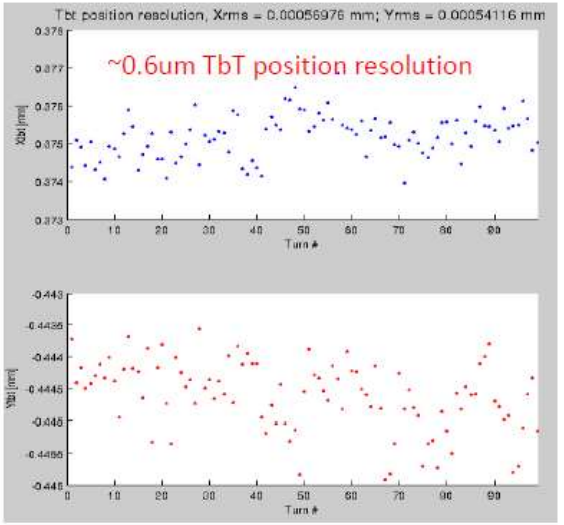
- Stable running several month
- Total memory size is 1 Gbyte
- Allocation memory logic side up to 300 Mbyte
- Linux system memory available up to 900 Mbyte
- CPU usage 20% user, 2.7 % system
- Free memory space is 770 Mbyte
- NSLS-2 operation, most diagnostics IOC need to support more than 35 client

Future plan based on zDFE and zynq U+ rfsoc

- Direct bunch to bunch measurement
- JESD204B 10Gbit serial interface and TBT, FA calculation
- 14-bit 4 channel 500 Mhz BxB BPM development (prototype coming soon)
- Beam tested with high speed ADC evaluation board (TBT 0.6um)







Summary

- NSLS-2 existing BPM hardware developed 2009 ~ 2011
- 2011 ~ 2014 Installed and commissioning the Linac/Booster/BTS injector and SR
- SR beam operation start since 2015 and stable operation

- RFBPM zDFE board is completed, and fully functional for NSLS-II application
- 10 Gbps transceivers will support future development for the BxB bpm.
- Improved performance use the CIC/FIR filter
- Use of Newer Xilinx/Vivado development environment and embedded epics IOC
- Installed zBPM prototype for performance measurement
- Expanded support for Pilot Tone(PT) signal processing for active calibration.
- Expanded application for the Cell controller, AI system, BxB BPM&Feedback system as well as beamline applications

Thank you for your attention!

Questions and comments are welcome.

V6 DFE board

- Virtex-6 FPGA
- Embedded MicroBlaze soft core processor running TCP/IP lwIP stack in conjunction with TEMAC Ethernet core
- 2Gbyte DDR3 SO-DIMM
- Memory throughput 6GBytes/sec
- (6) 6.5Gbps SFP modules
- Fixed Point DSP Engine
- 1Gbit FLASH memory
- Embedded Event Receiver

DFE also serves as :

Cell Controller for Fast Orbit Feedback

AI system for Fast machine protection

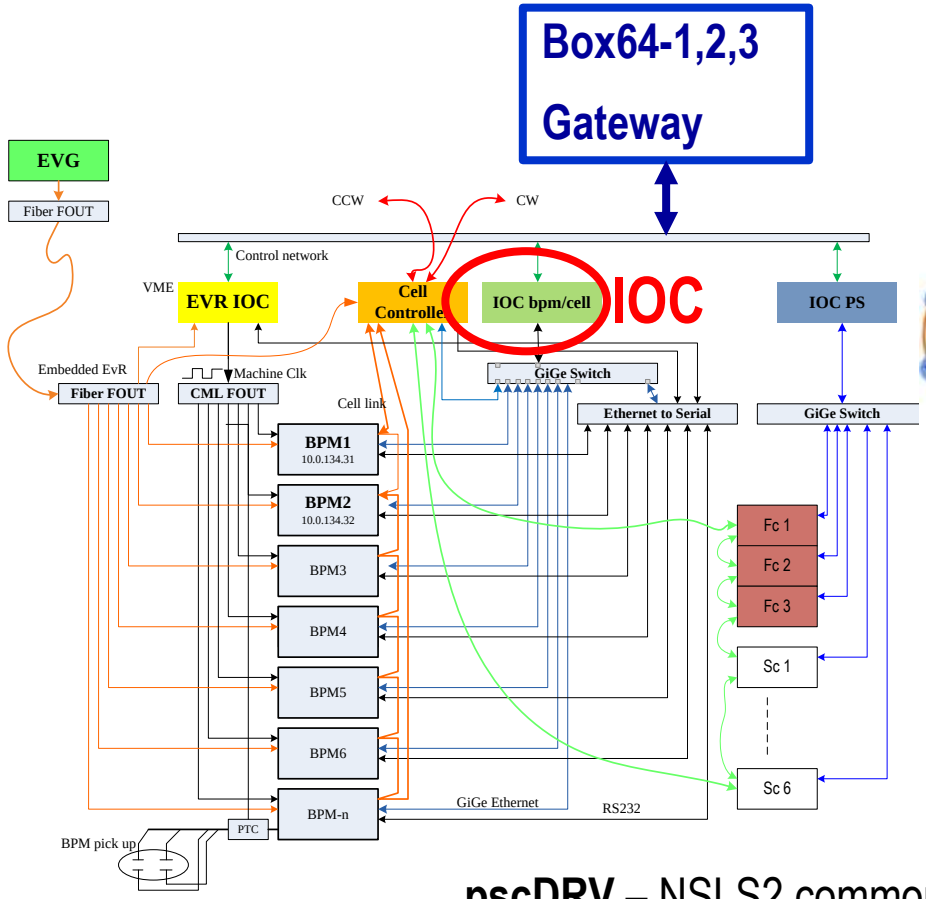
NSLS-II BPM

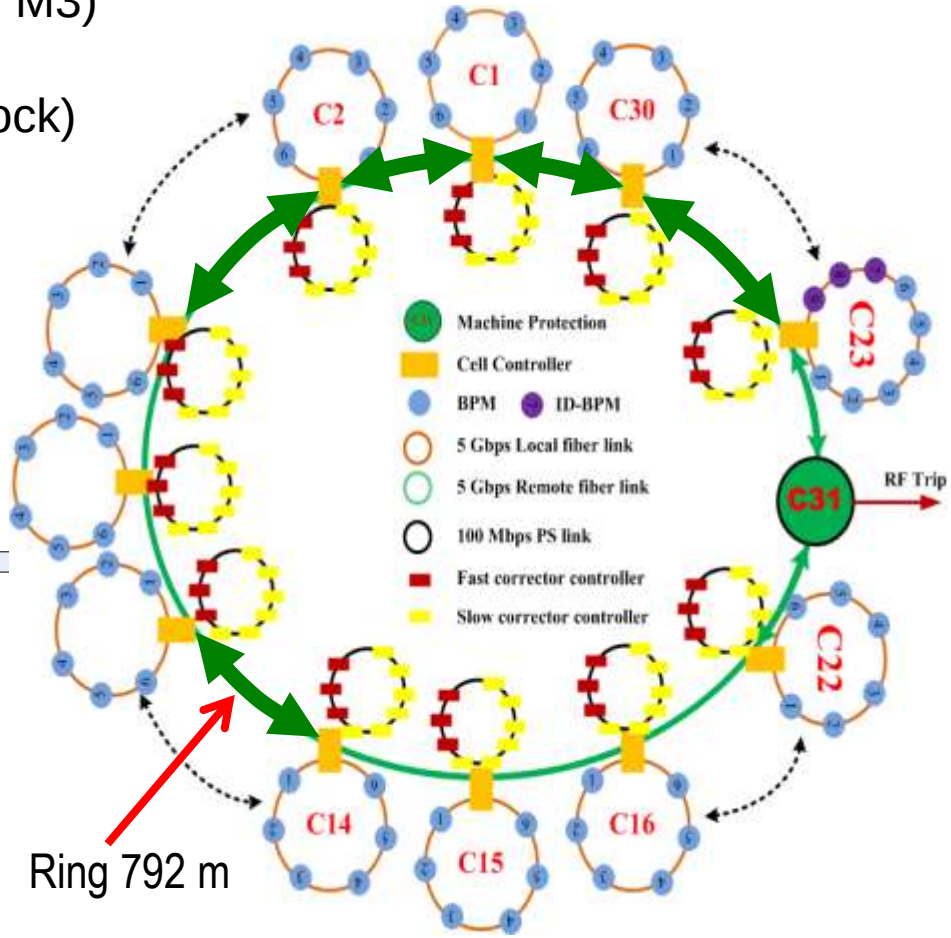
Data Type	Mode	Max Length
ADC Data	On-demand	256Mbytes or 32M samples per channel simultaneously
Turn-by-Turn (TbT), Frev=379 kHz	On-demand	256Mbytes or 5 M samples Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
Fast Acquisition (FA) , 10KHz	Streaming via SDI Link & on demand	Streaming - X,Y,SUM; For on demand: 256 Mbytes or 5 Msamples. Va,Vb,Vc,Vd, X,Y, SUM, Q, pt_va,pt_vb,pt_vc,pt_vd
Slow Acquisition (SA), 10Hz	Streaming and On-demand	80hr circular buffer Va,Vb,Vc,Vd, X,Y,SUM, Q, pt_va,pt_vb,pt_vc,pt_vd

- Development started August 2009
- First Beam Test at LBNL on ALS June 2010
- All requirements demonstrated February 2011
- Booster complete March 2012
- Storage Ring complete June 2013
- SR commissioning complete May 2014

Global hardware system configuration

- 3 tier network configuration
- 30 diagnostics IOCs(IBM System x3550 M3)
- 30 Cell Controller (FOFB)
- 1 Fast Machine protection (Active Interlock)





pscDRV – NSLS2 common IOC for the FPGA communication