IBM Research

Investigating the future of nano-electronics using x-rays

Conal E. Murray

2015 SRI Satellite Workshop

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Acknowledgments

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- S. Hruszkewycz
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Outline

Evolution of CMOS technology

- micro → nano
- when scaling breaks down

Present challenges

- dopant distribution
  - contact resistance
  - electromigration
- strain engineering
  - mobility

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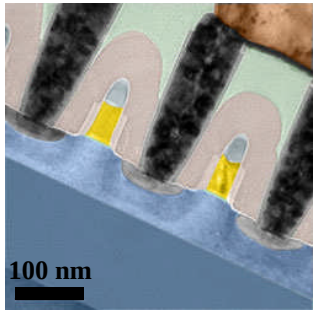
Motivation

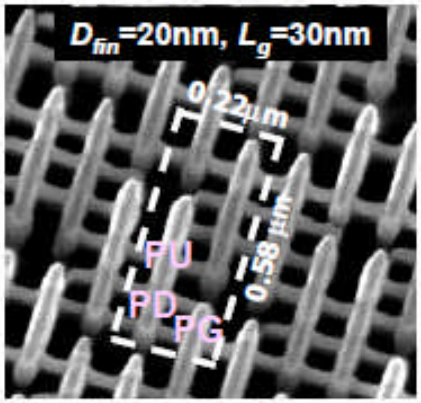
Nanomaterials:

- new properties enabled by increasing surface to volume ratio
  - strength
  - electronic behavior
  - <u>interfaces are everywhere</u>

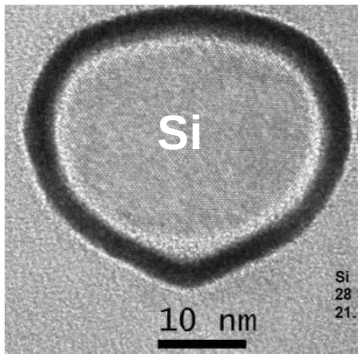
- semiconductor device scaling
  - ✓ increased density
  - ✗ lithographic scaling is no longer sufficient in improving device performance

  - new materials and <u>geometries</u> must be incorporated





H. Kawasaki et al., IEEE IEDM 12.1 (2009)



L. Gignac et al., FIB User's Group Meeting, NIST (2010)

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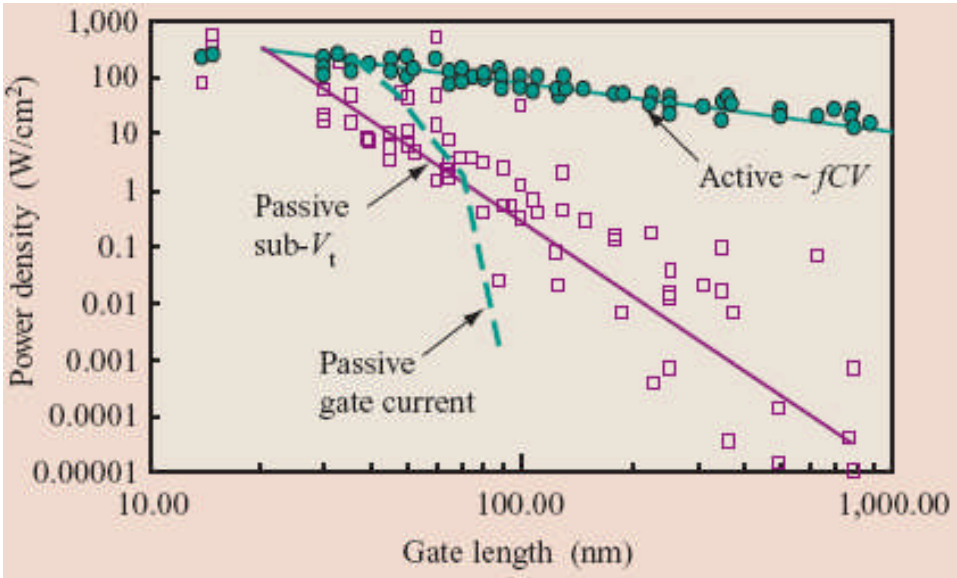
End of Classical CMOS scaling

Deviation from "ideal" scaling

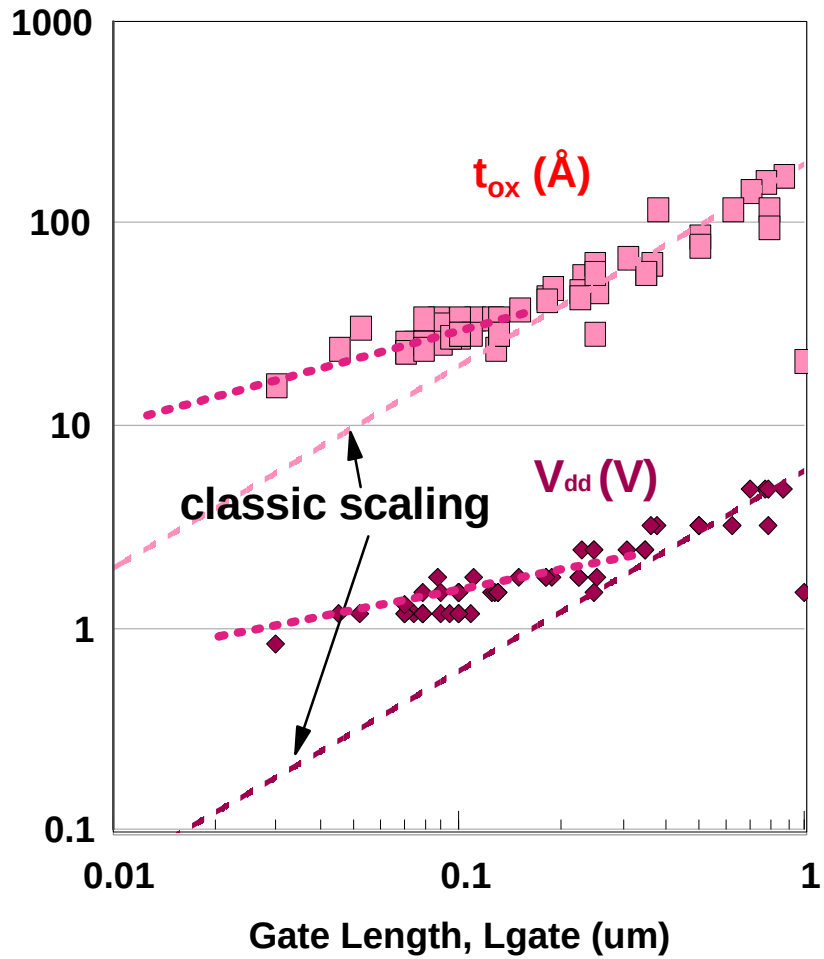
- thinner insulation → increased gate leakage
- lower voltage → less performance

Consequence of these deviations?

- **dramatic rise in power density**



W. Haensch et al., IBM J. Res. Dev. **50,** 339 (2006)



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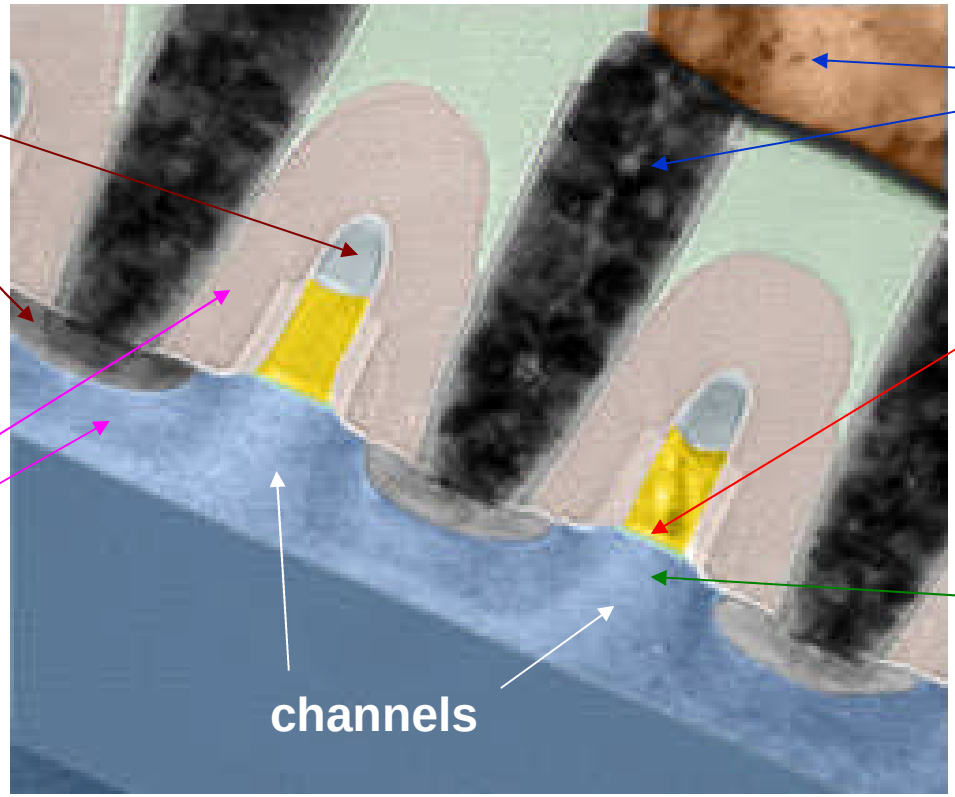
Future needs of nanoelectronics characterization

Many material and structural issues exist to enhance device performance:

- strained Si channels lead to enhanced carrier mobility in devices
- composition, phase transitions, and microstructure of device components
- mechanical behavior and interfacial scattering within devices



silicide (NiPt)

metallization (Cu,W,Al)

gate dielectric (SiO_2, high-K)

stressor materials (Si_3N_4, SiGe, SiC)

dopants (As, P, B)

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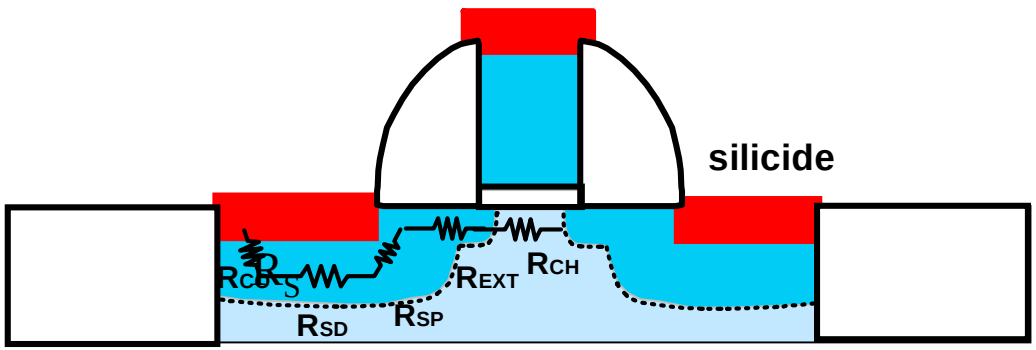
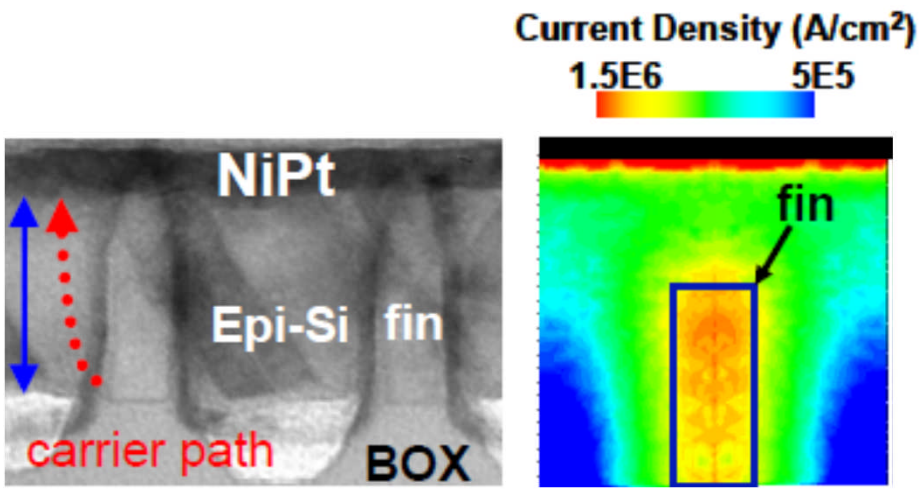
Contact metallization: Self-Aligned silicides

Lower Total Source-Drain Resistance → Higher Drive Current Faster Devices



R_{CH} = channel resistance
R_{SD} = sheet resistance in S/D
R_{SP} = spreading resistance
R_{EXT} = Sheet resistance in extensions
R_{CO} = silicide/silicon contact resistance



H. Kawasaki et al., IEEE IEDM 12.1 (2009)

$$R_{CO} \sim \exp\left[(\Phi_B) / (N_d)^{1/2} \right]$$

Φ_B : Schottky barrier height
N_d : Dopant density

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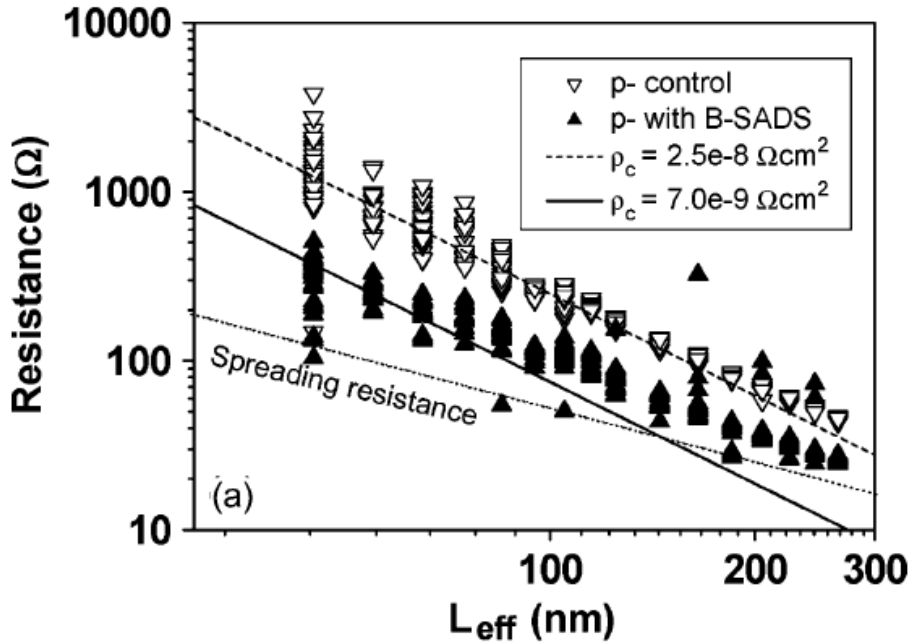
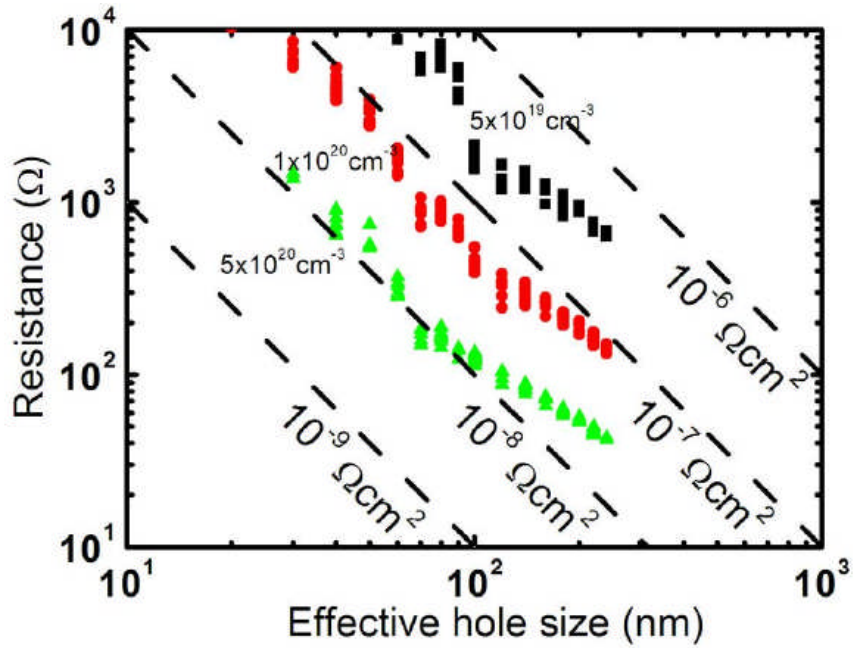
Effects of dopant density on contact resistance



Z. Zhang et al., IEEE EDL, **31**, 731 (2010)



K. Ohuchi et al., IEEE IEDM, 1029 (2007)

- interfacial density of dopants critical to reducing contact resistance

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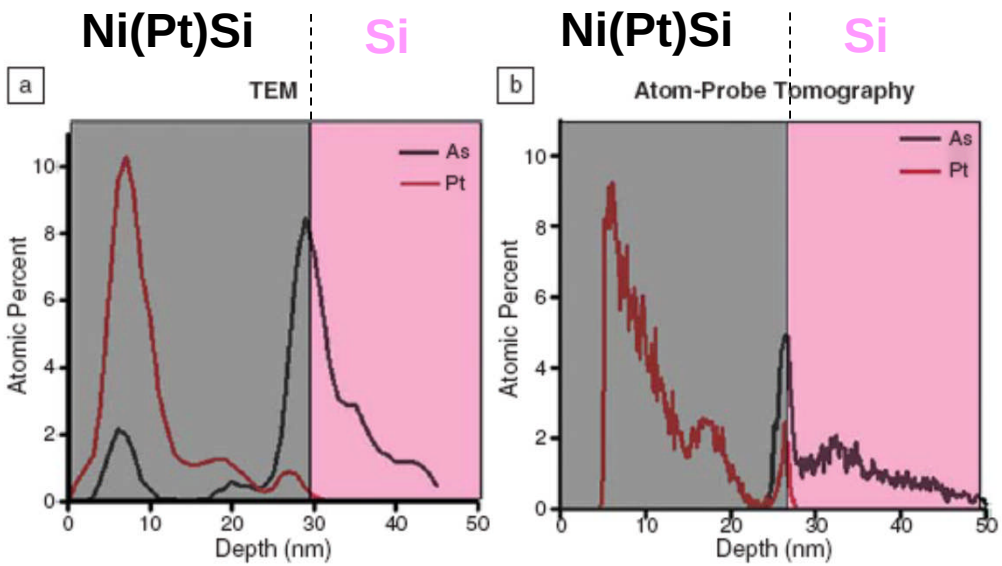
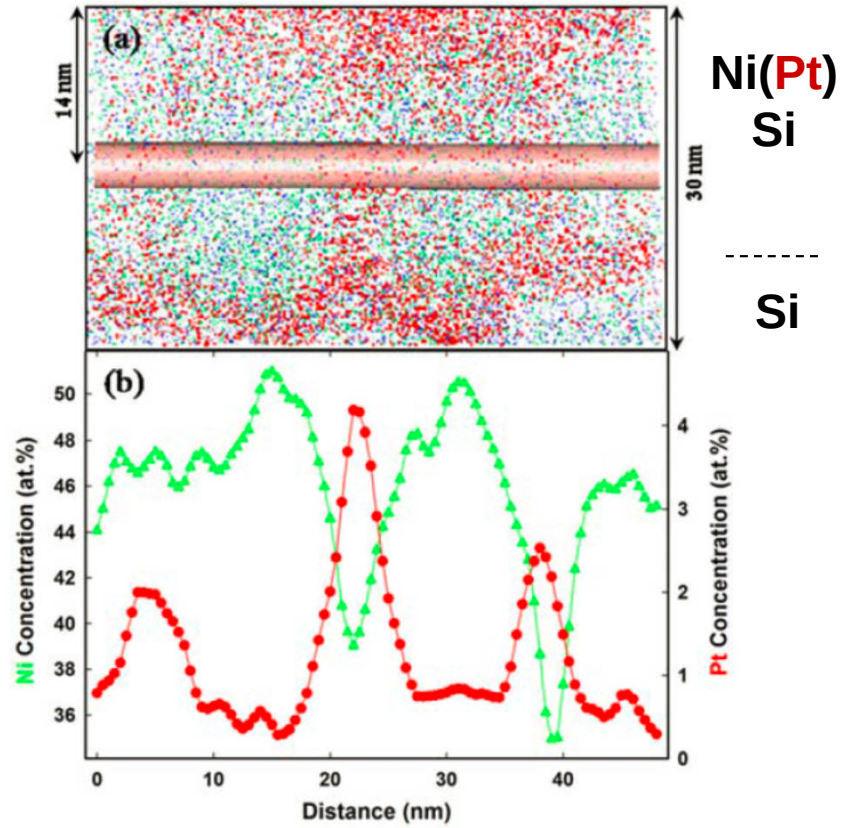
Investigating dopants in contact materials (ex-situ)



P. Ronshiem et al., MRS Bulletin, **34**, 739 (2009)



P. Adusumilli et al., JAP, **112**, 064307 (2012)

- microstructure impacts dopant locations
  - assess Pt bonding states at interfaces / grain boundaries

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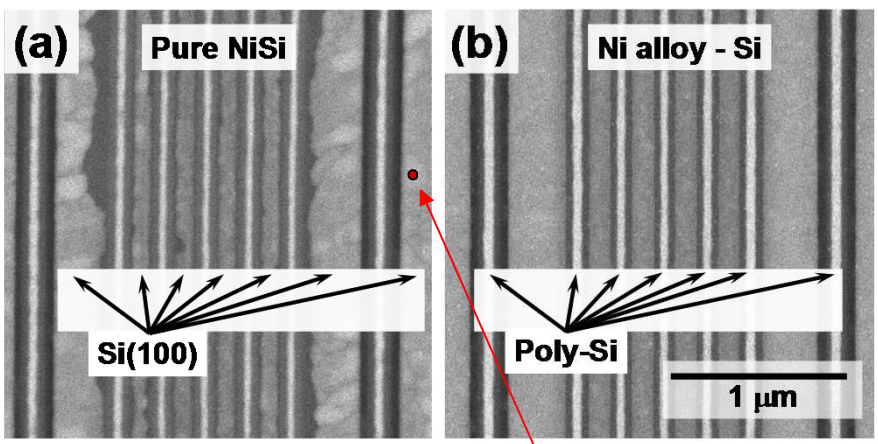
Incorporation of alloying elements into Ni silicide

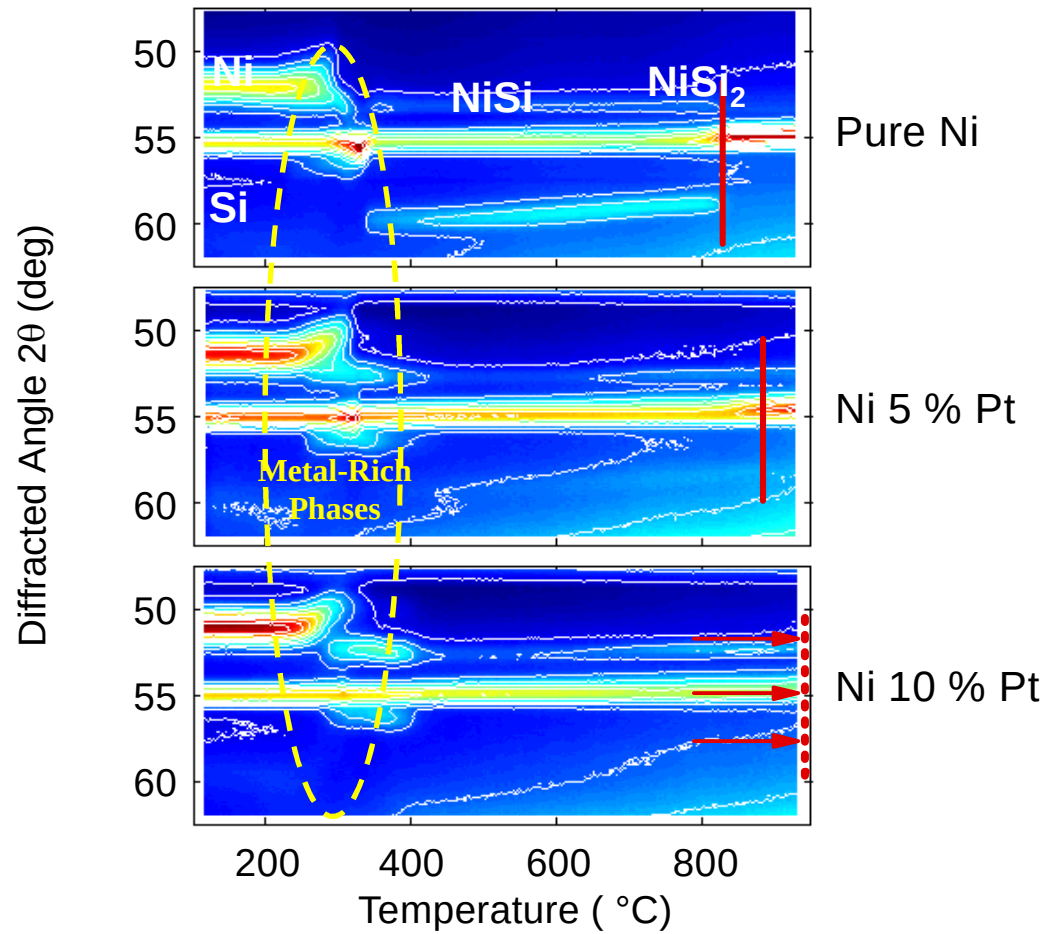
Ni(Pt)Si alloying:

- limits metal-rich phases
- retards $NiSi_2$ formation
- delays agglomeration
- changes monosilicide texture



- as contact dimensions decrease, grain size → contact area

In-situ XRD



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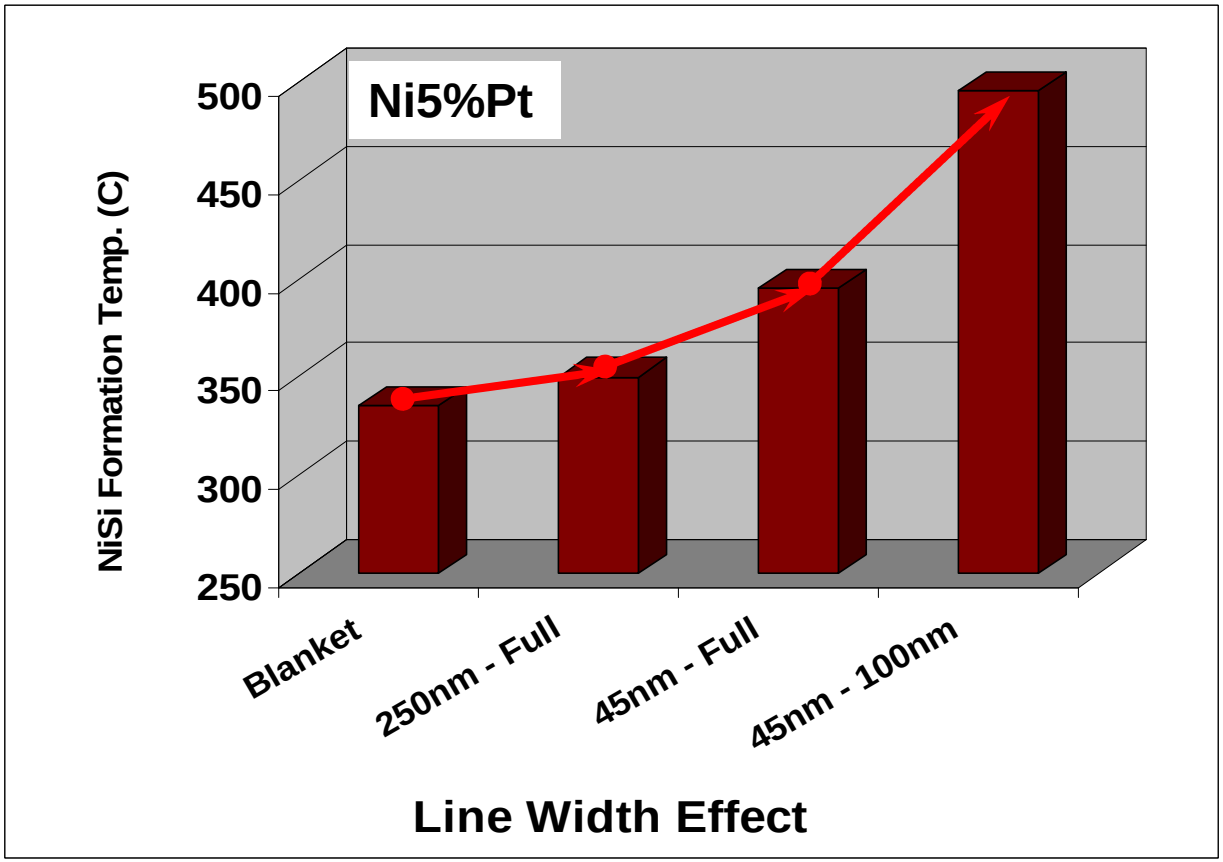
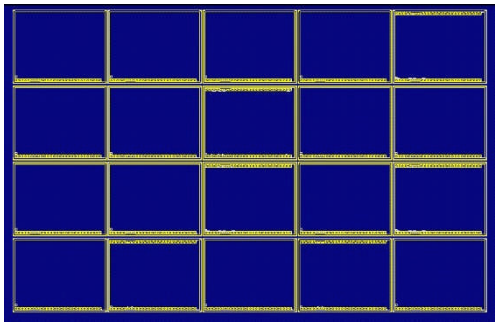
Silicide formation temperature vs. feature size



Formation Temperature:

- **Ni (5% Pt) shows a strong dependence on feature size**

Maskset



- XRD measurements conducted on arrays of features (4 x 4.8 mm regions)
  - need to analyze individual features

C. Lavoie et al., Denver X-ray Conference (2010)

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History of the transistor

- Ge point contact transistor (1947)
  - also Si*

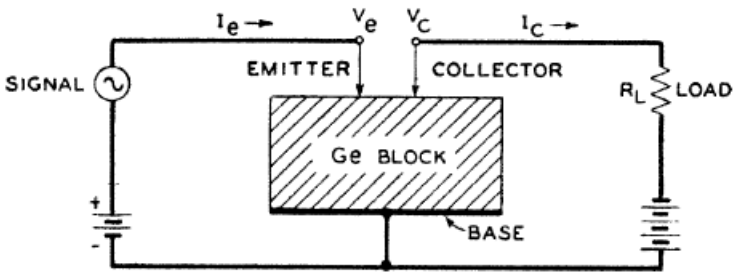
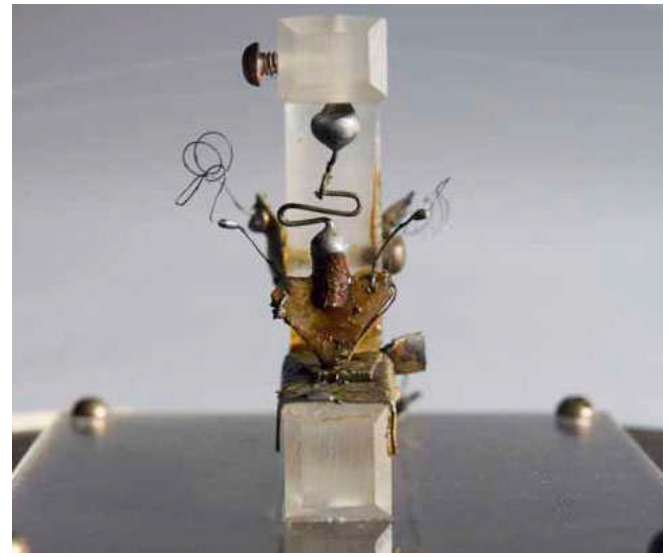
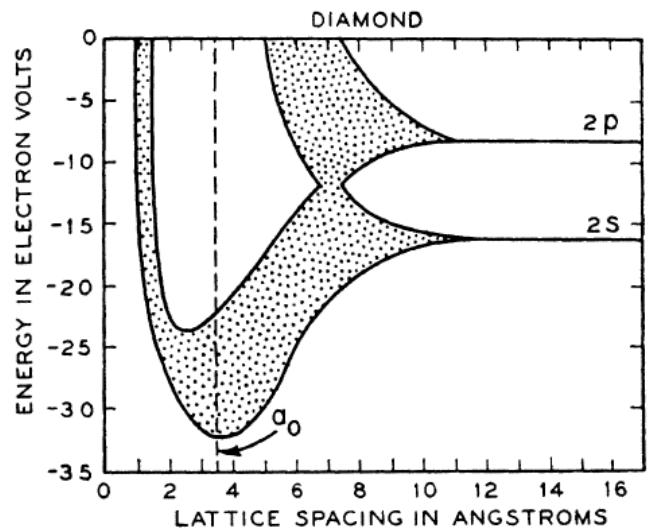


FIG. 1. Schematic of semi-conductor triode.

*J. Bardeen and W.H. Brattain, Phys. Rev. **78,** 230 (1948)

- Effects of semiconductor deformation
  - bandgap
  - effective mass
  - primarily dilatation (hydrostatic)





J. Bardeen and W. Shockley, Phys. Rev. **80,** 72 (1950)

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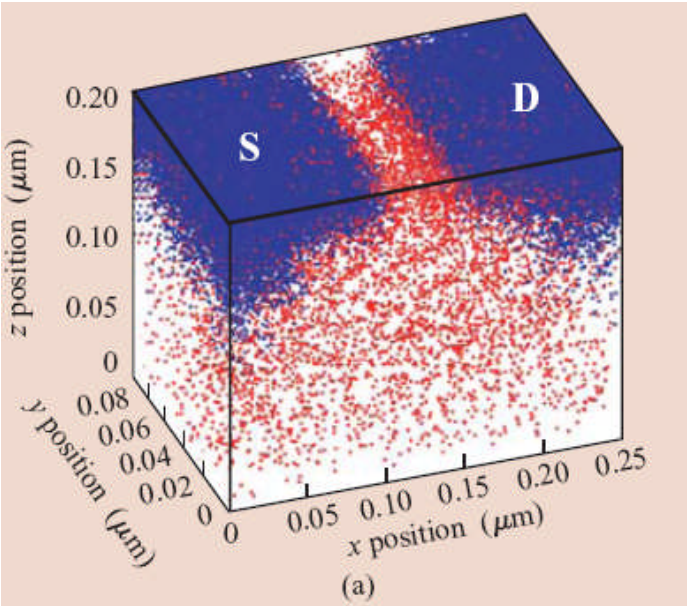
Device channel scaling

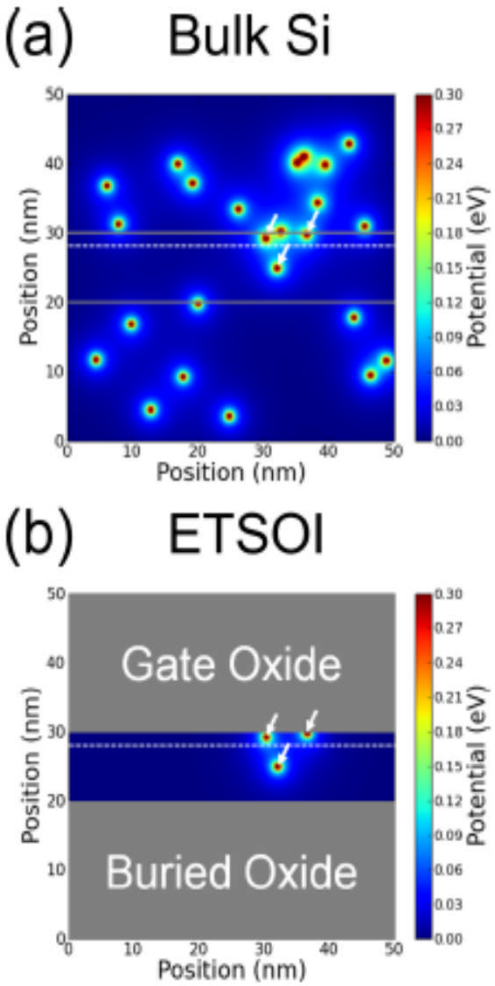
- variation in device behavior due to dopant distributions

- short channel effects
  - ➢ thinner active Si (ETSOI)



K. Bernstein et al. IBM J. Res. Dev. **50**, 0018-8646 (2006)

random dopant fluctuations
- ➢ big impact on thinner devices



N. Kadotani et al. J. Appl. Phys. **110**, 034502 (2011)

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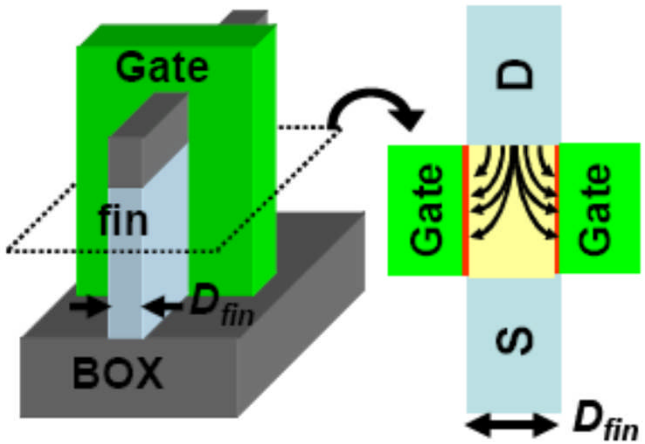
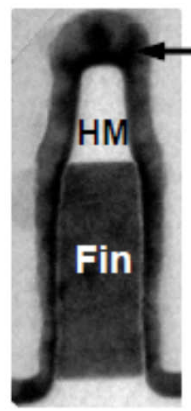
3D device architecture: FinFET





The thickness of HKMG should be uniform along fin height.

source of σV_t	origin
T_{ox} variation	non-uniform thickness of HK
ε_{ox} variation	non-uniform composition of HK
WF variation	non-uniformity of MG
	grain size variation
	multi-surface orientations
charges	traps and states

H. Kawasaki et al., IEEE IEDM 12.1 (2009)

- Gate encapsulation → better electrostatic control
- lower threshold voltages → less power
- device behavior dominated by fin interface

<u>challenges</u>

- 3D strain distribution (SiGe and gate effects)
- uniformity of high-k dielectric / metal gate (HKMG) layers
- thickness, composition, grain size / orientation

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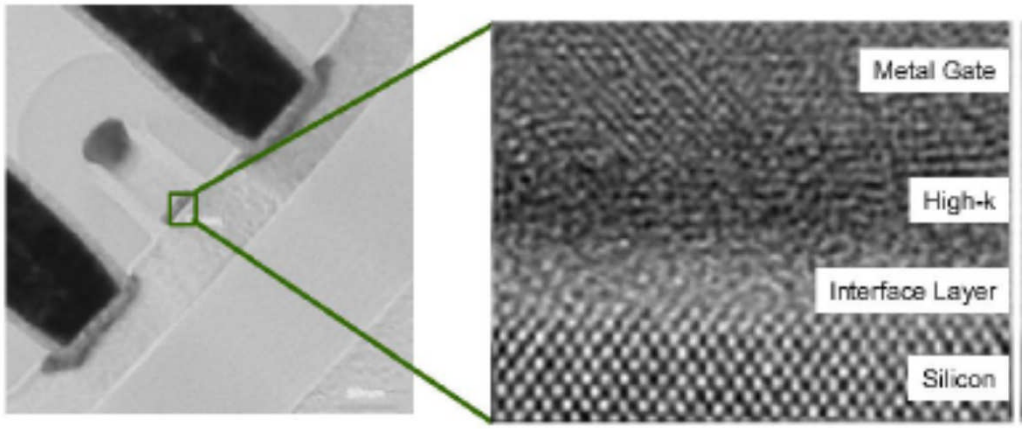
High-k dielectrics

- SiOx gate dielectric scaling
  tunneling → breakdown

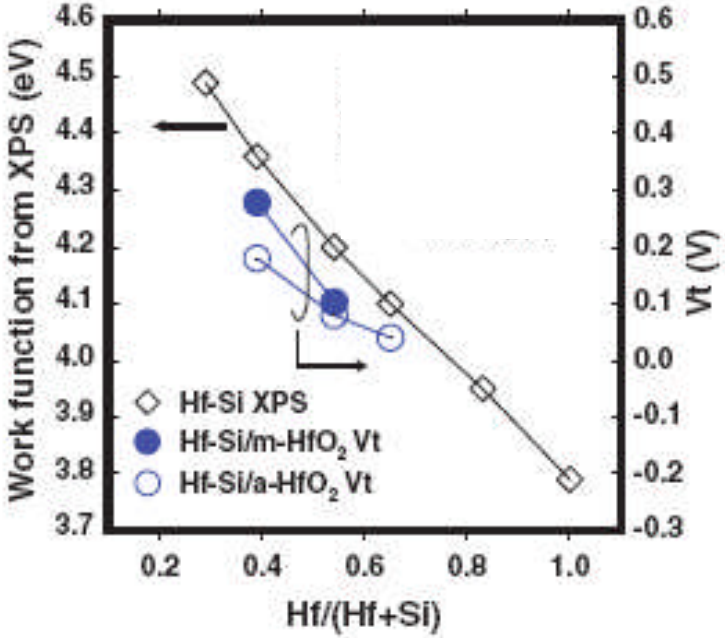
- Reduce leakage current by
  employing high-k materials



M. Khare, IEEE CICC 15-3 (2007)

- variation in device behavior
  - ➢ Hf, O content impacts work function

- can chemical state be determined?
  - ➢ spatially-resolved XANES



T. Ando et al., Appl. Phys. Express 2 (2009) 071402

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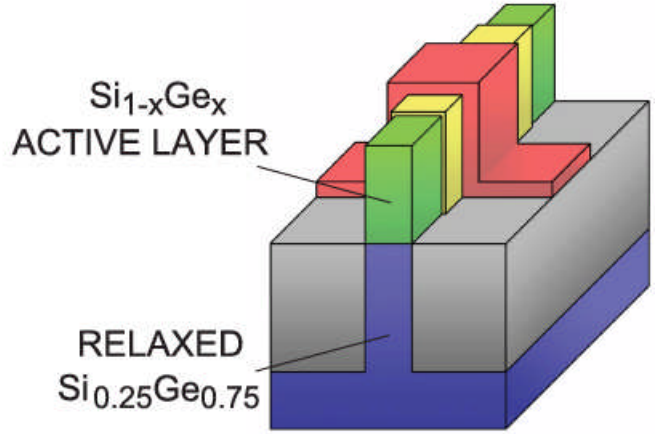
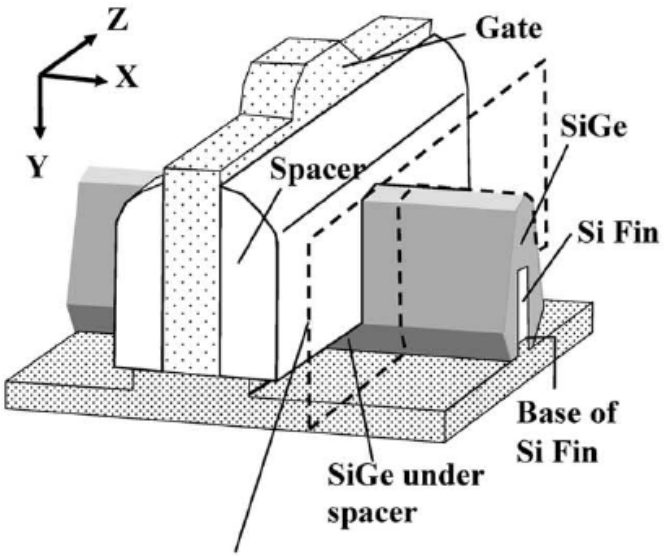
Strain in FinFET devices

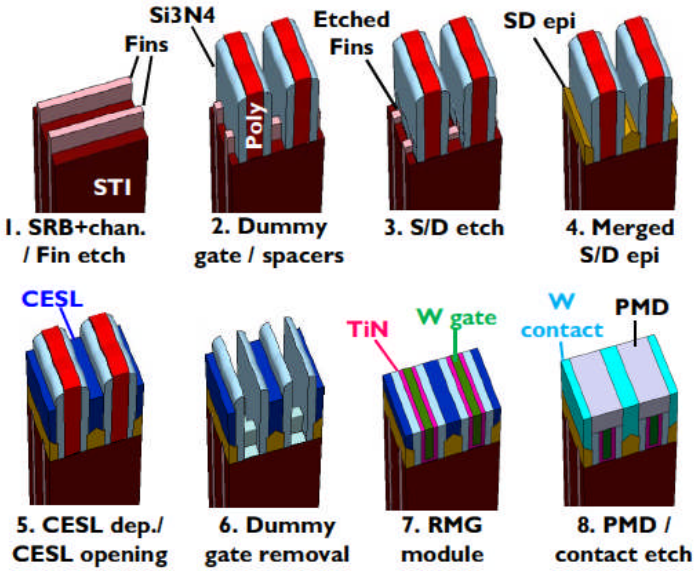
- greater elastic compliance
  - ➢ wrap-around stressors
- "uniaxial" fin stress
- ➢ ALL structures must be considered !



D. Lizzit et al., IEEE TED **60**, 1884 (2013)



K-M Tan et al., IEEE EDL **28**, 905 (2007)



G. Eneman et al., IEEE IEDM 6.5.1 (2012)

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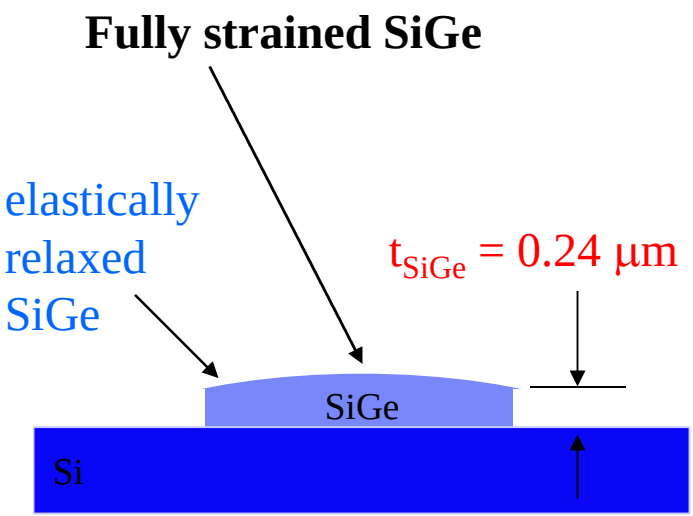
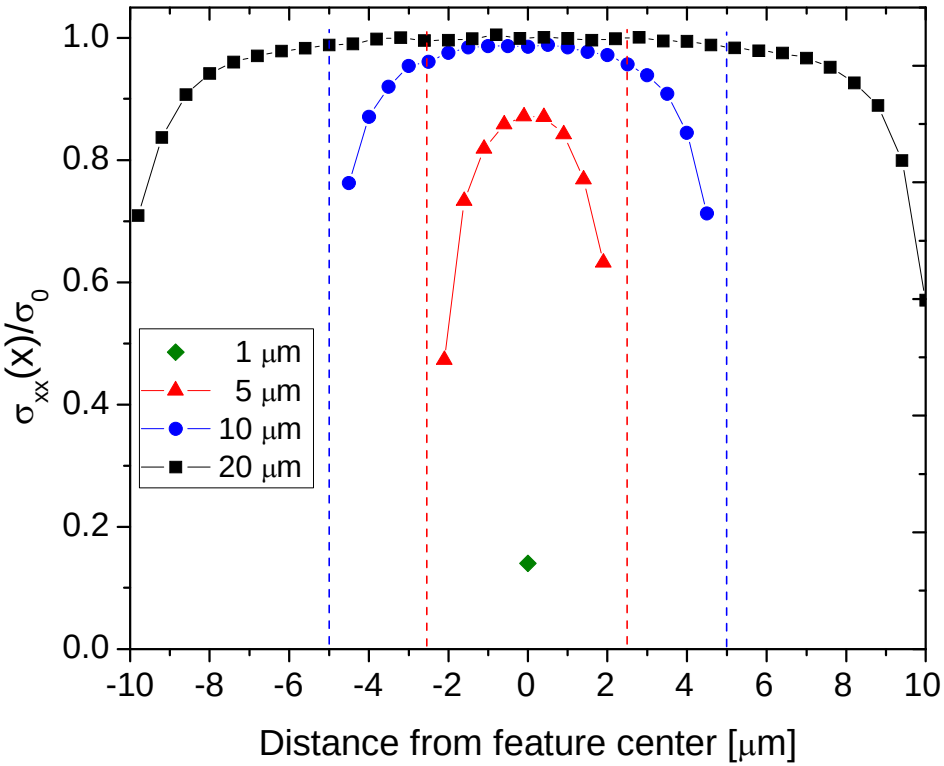
Results: strain mapping across SiGe features





- scanning Bragg diffraction (2-ID-D: 0.25 μm FWHM @ 11.2 keV)
- strain reduction at SiGe feature center for features < 10 μm width
  - elastic relaxation extends ~ 20 t_{SiGe} from edge

C.E. Murray et al., J. Appl. Phys. **98**, 013504 (2005)

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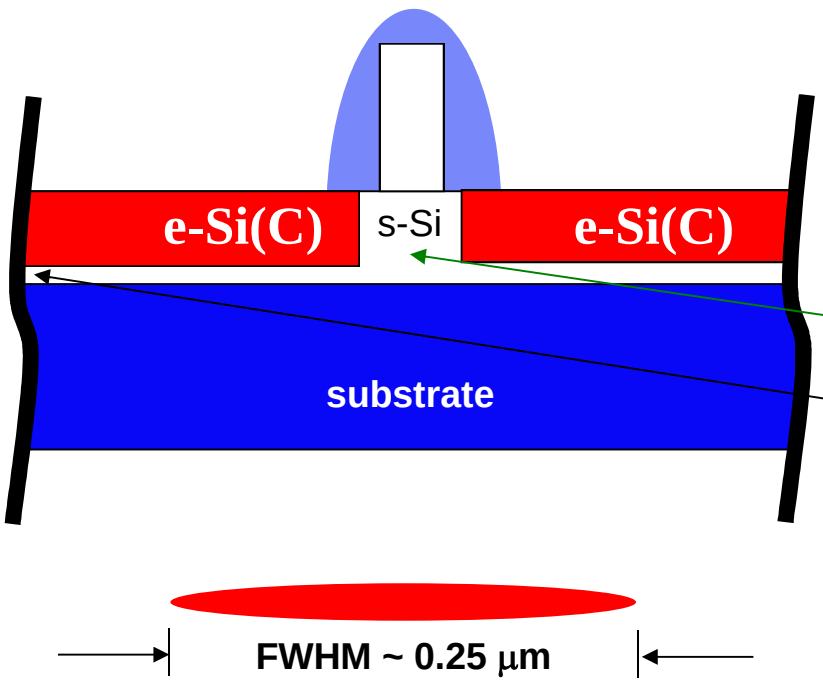
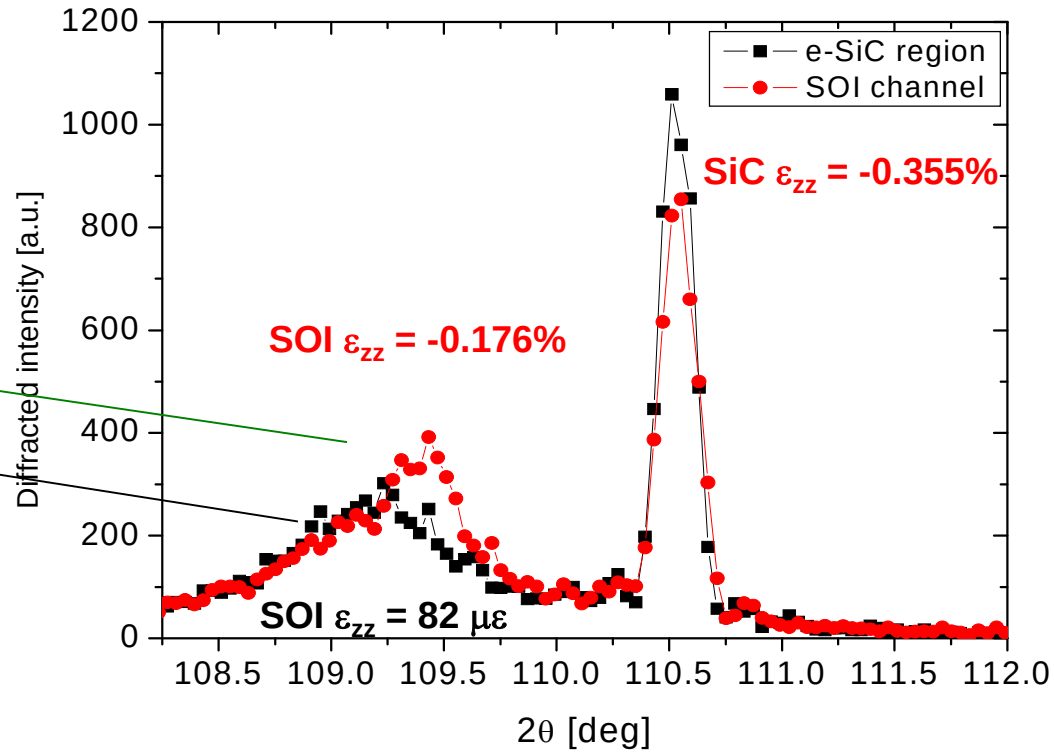
Strain in SOI channel due to embedded features

- measured e-Si(C) strain is equivalent near SOI channel and ~ 1 μm from channel
  - lower intensity due to presence of SOI in channel
- greater SOI strain in channel region than under e-SiC features
  - small SOI strain under e-SiC





C.E. Murray et al., Appl. Phys. Lett. **94**, 063502 (2009)

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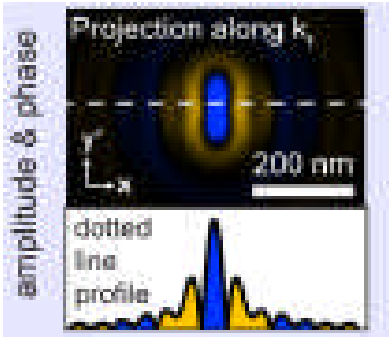
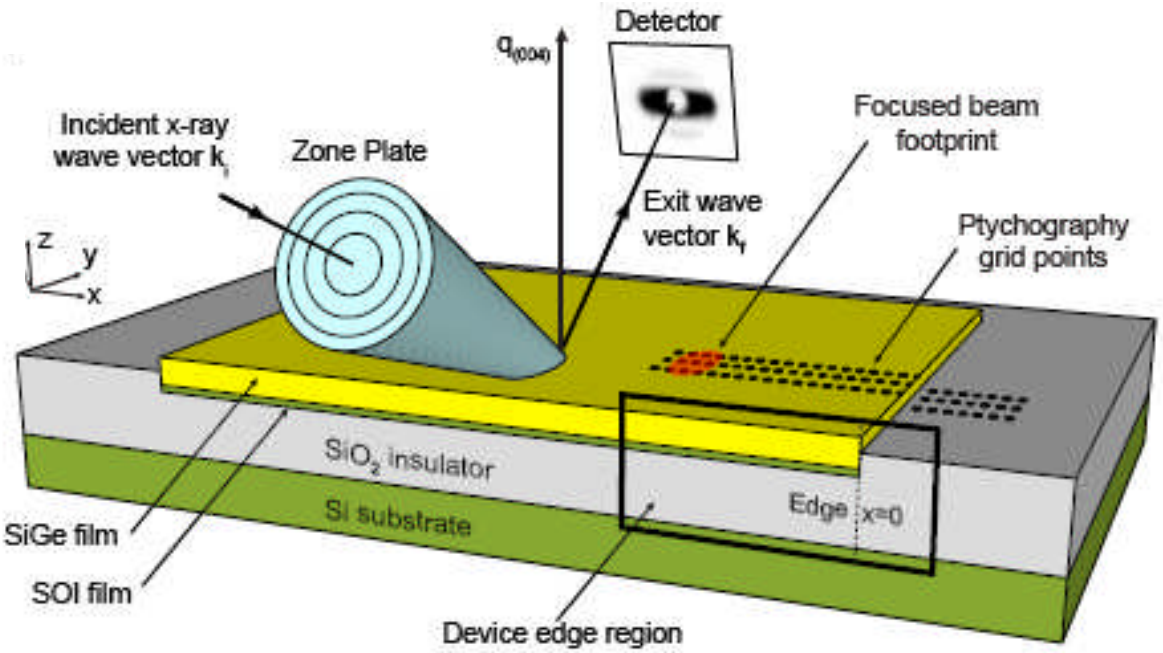
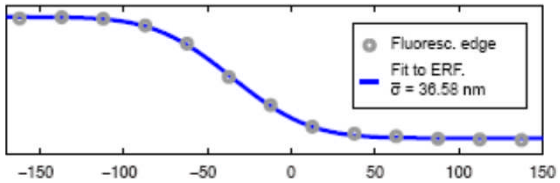
Bragg Projection Ptychography (BPP)

- based on coherent diffractive imaging (CDI)
- selective oversampling of (004) diffraction information
- reconstruction of lattice and incident beam
- ➢ resolution less than incident beam size (85 nm FWHM) →





Ge Kα fluorescence



S. Hruskewycz et al., NanoLett. **12**, 5148 (2012)

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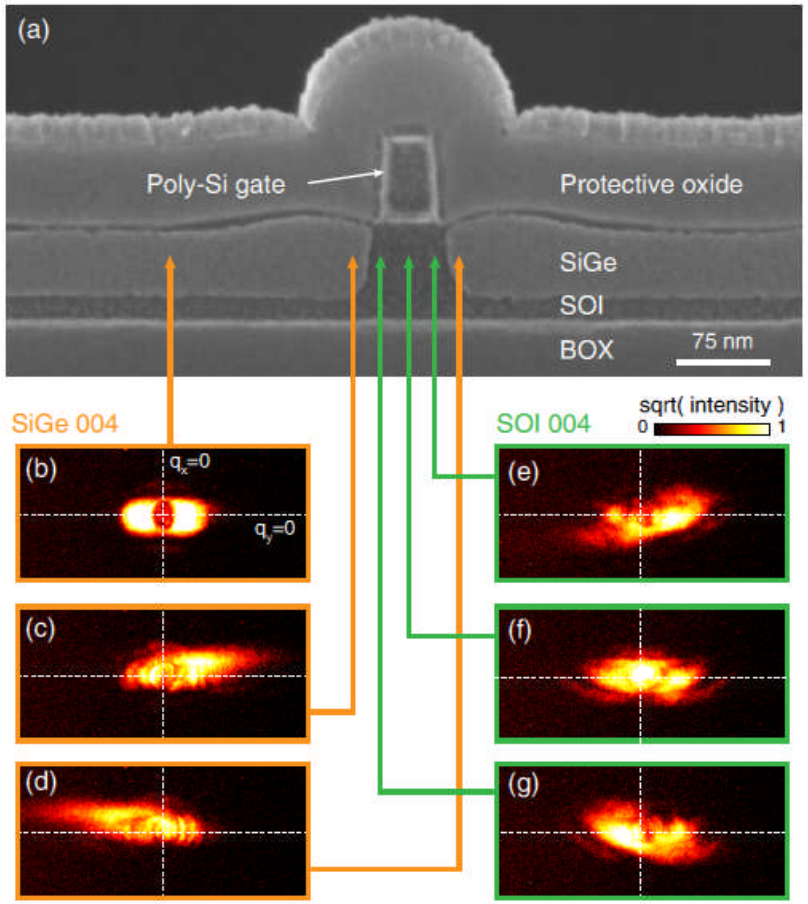
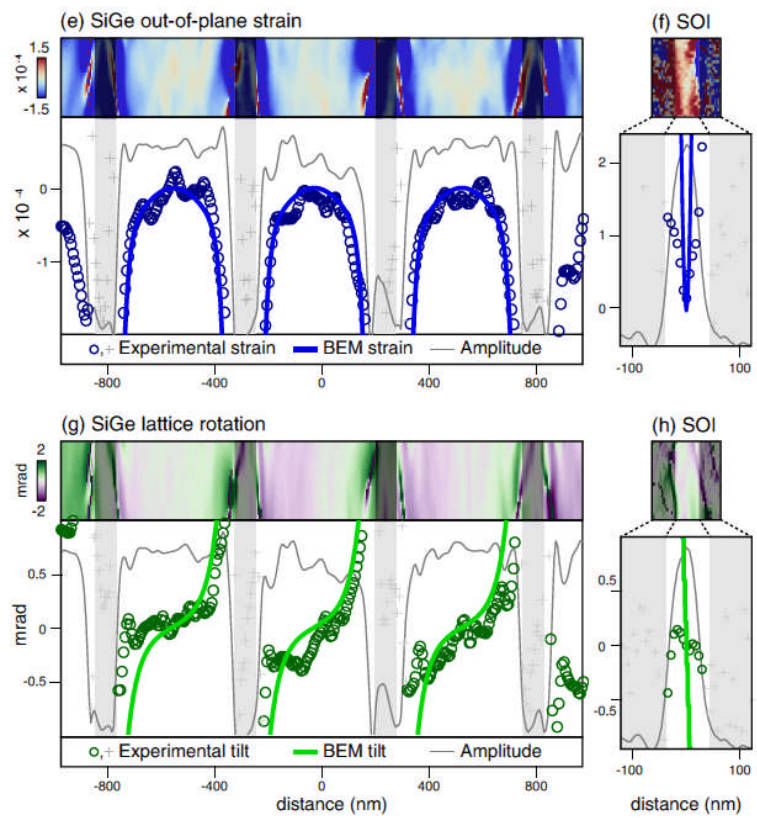
Results: e-SiGe stressors on device channels (26ID)

Strained-SOI channels



M.V. Holt et al., Phys. Rev. Lett. **112**, 165502 (2014)

- extraction of strain and lattice tilt
- ➢ probe defect behavior (dislocations, stacking faults)



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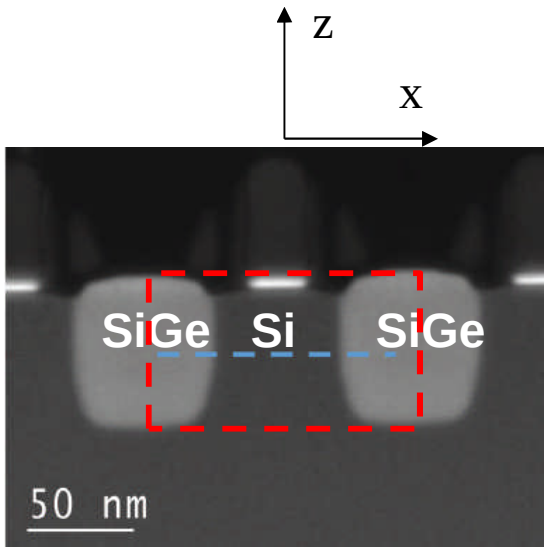
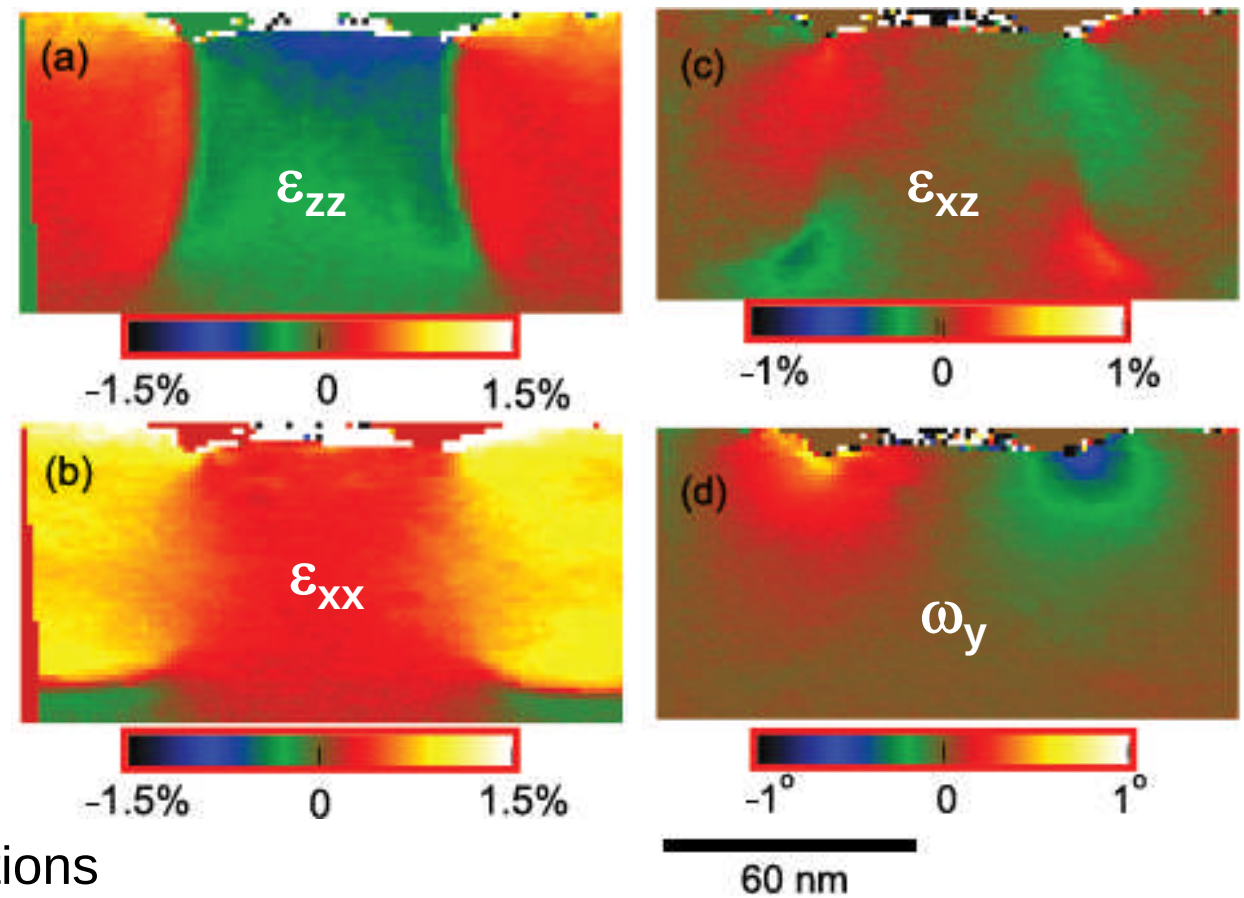
Electron diffraction strain measurements (PED)

"Depth-dependent" deformation in strained-Si / SiGe structures





- GPA from multiple reflections
- ~ 3 - 5 nm spatial resolution

Y.Y. Yang et al., Appl. Phys. Lett. **106**, 042104 (2015)

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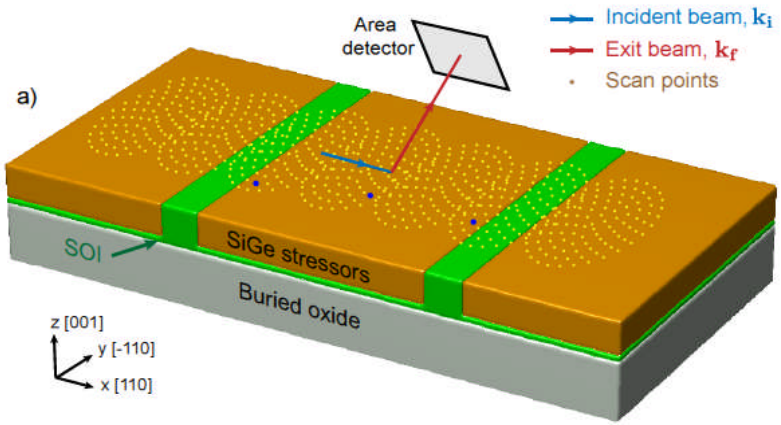
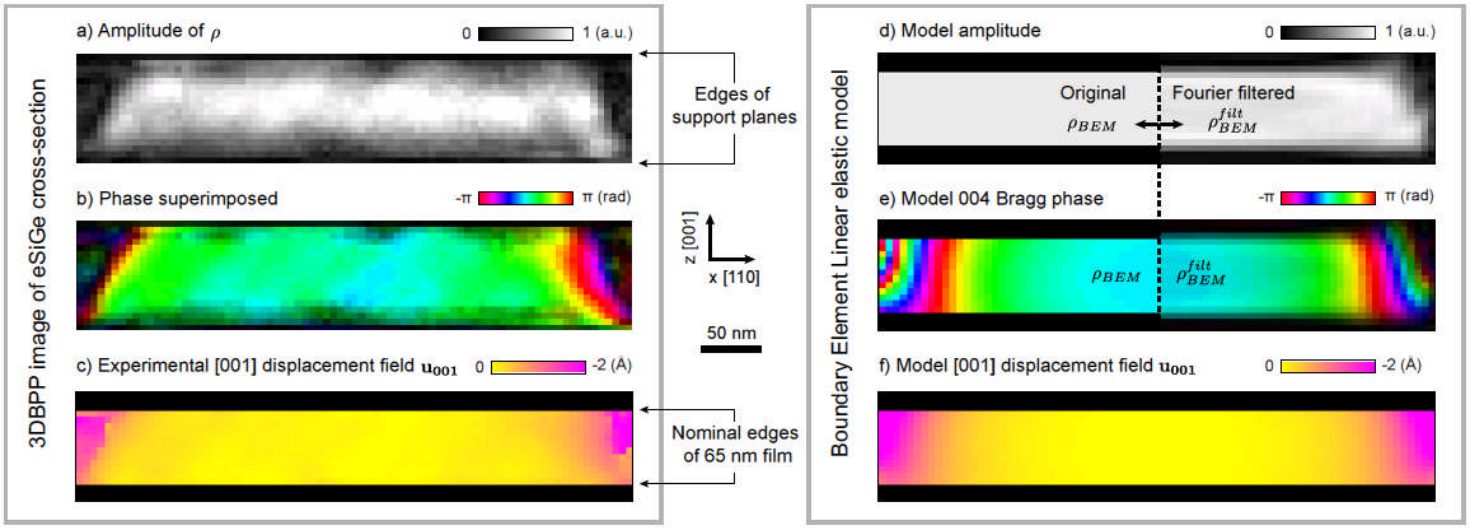
3D BPP

- Reconstruct 3D strain distributions in e-SiGe stressors and SOI channels





S.O. Hruszkewycz et al., ArXiv 1506.01262 (2015)

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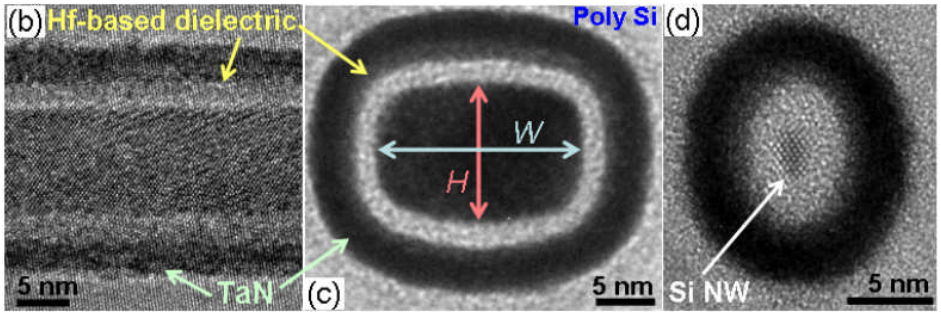
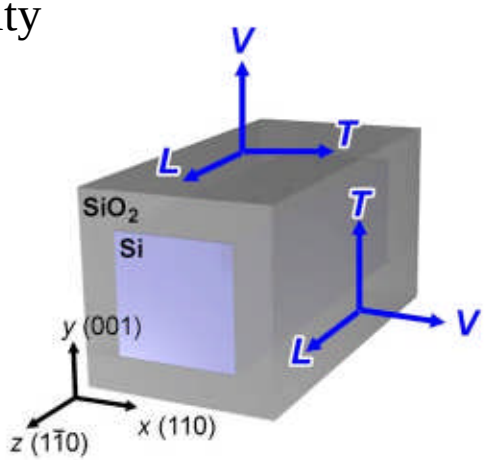
Nanowires

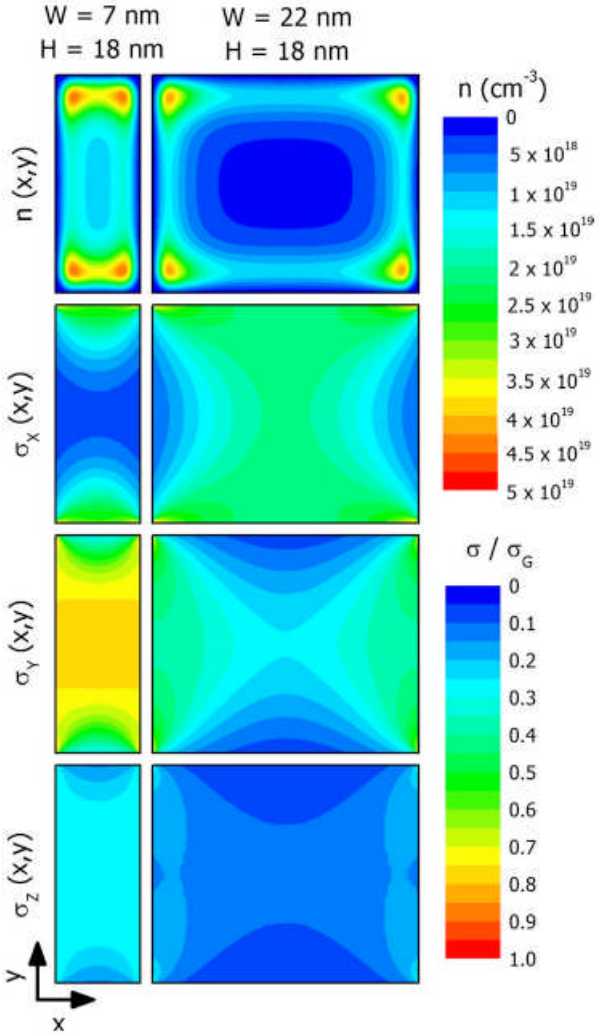
- full encapsulation of active region (GAA)



S. Bangsaruntip et al., VLSI Symp. 21, (2010)

➢ convolution of stress distributions and carrier density





L. Sekaric et al., Appl. Phys. Lett. **95**, 023113 (2009)

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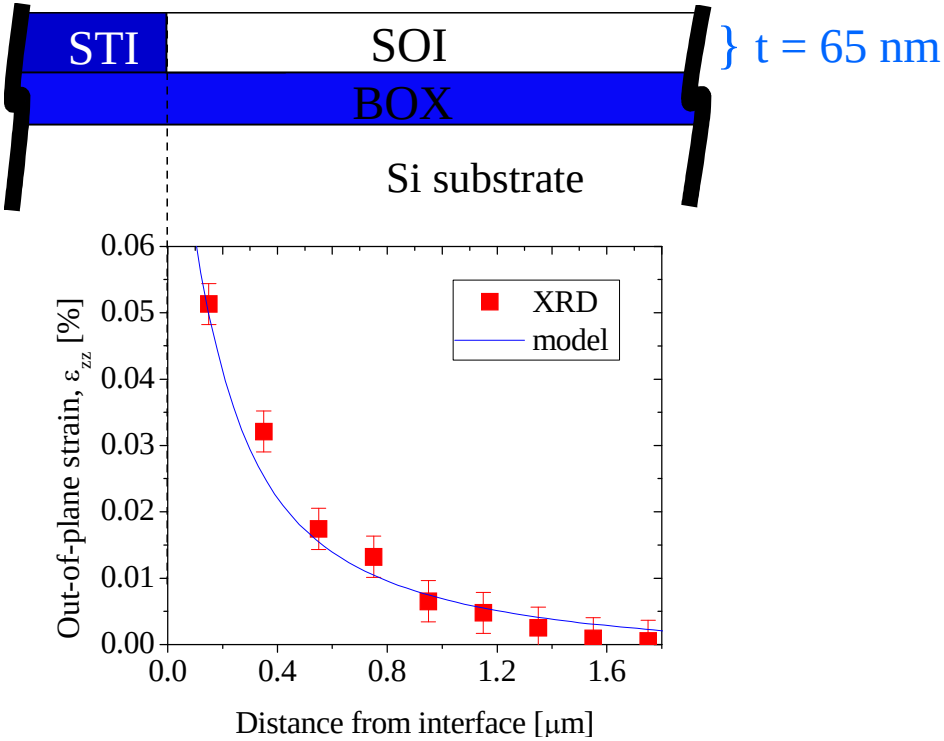
Impact of adjacent stressors on device strain

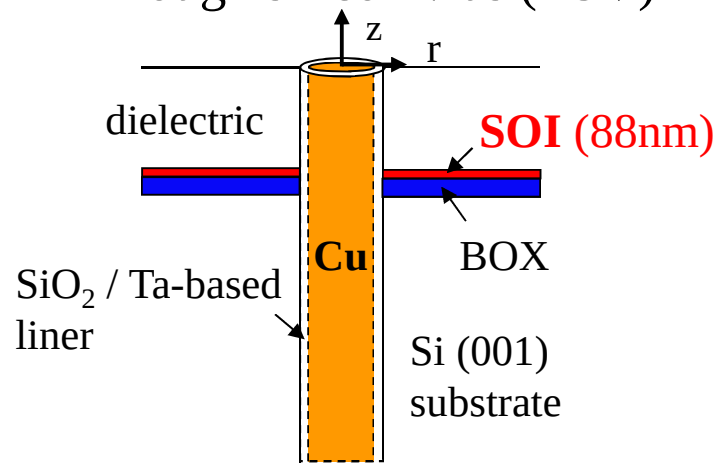
- Shallow trench isolation (STI)

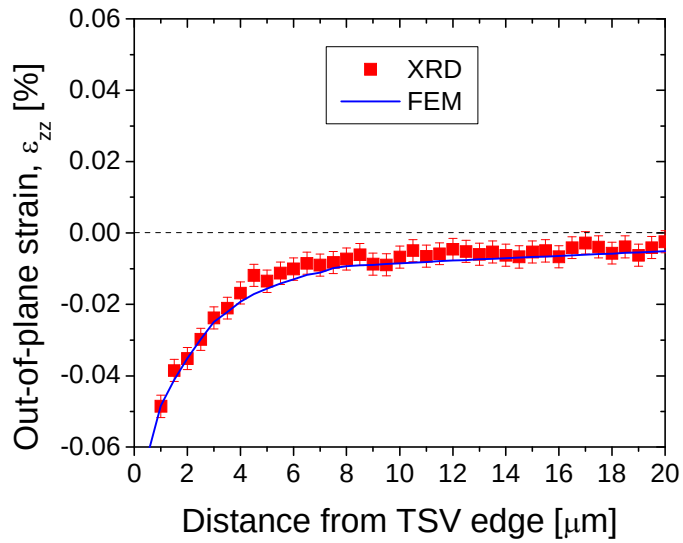


➢ effects extend ~ 25 x thickness

C.E. Murray et al., Appl. Phys. Lett. **90**, 171919 (2007)

- Through silicon vias (TSV)





C.E. Murray et al., Appl. Phys. Lett. **102**, 251910 (2013)

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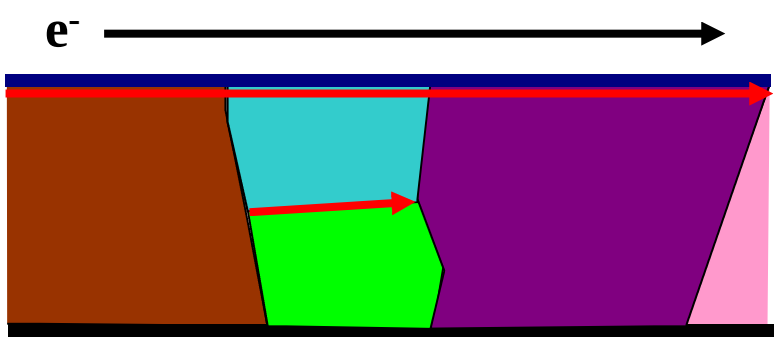
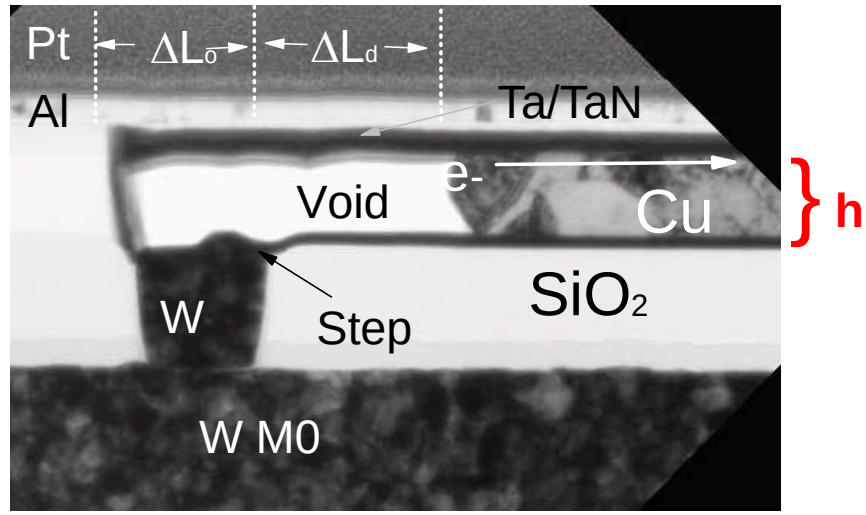
Electromigration

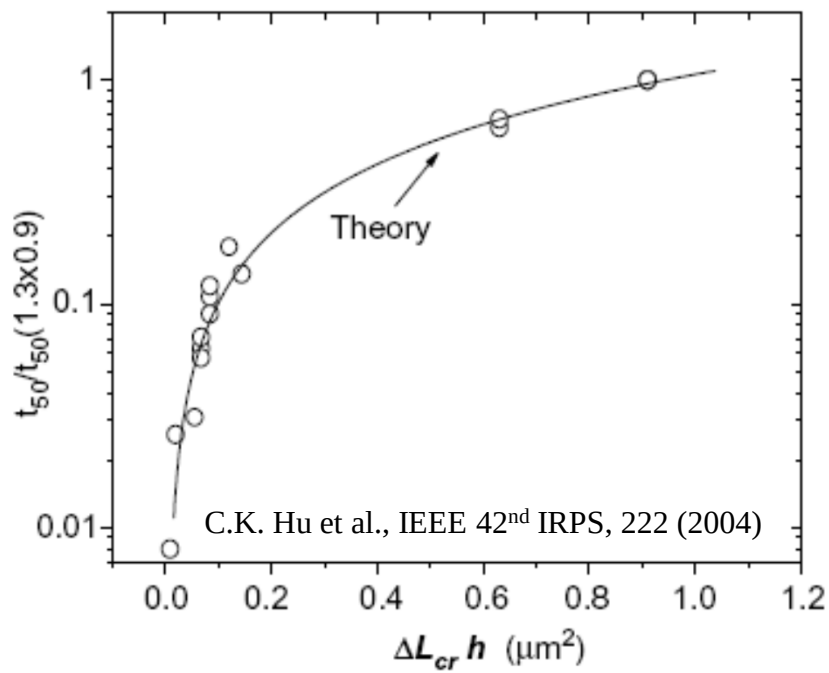
- **Flow of atoms due to electronic "wind force"**
- **Depletion of interconnect leads to voids**
  - flux divergence points most susceptible
- **Current density increases with scaling**
  - median lifetime (t_{50}) halves per generation

$$t_{50} = \frac{\Delta L_{cr}}{v_d} \propto \Delta L_{cr} h$$

- **Microstructure impacts electromigration**
  - grain boundaries parallel to current flow
  - interfaces (top surface)







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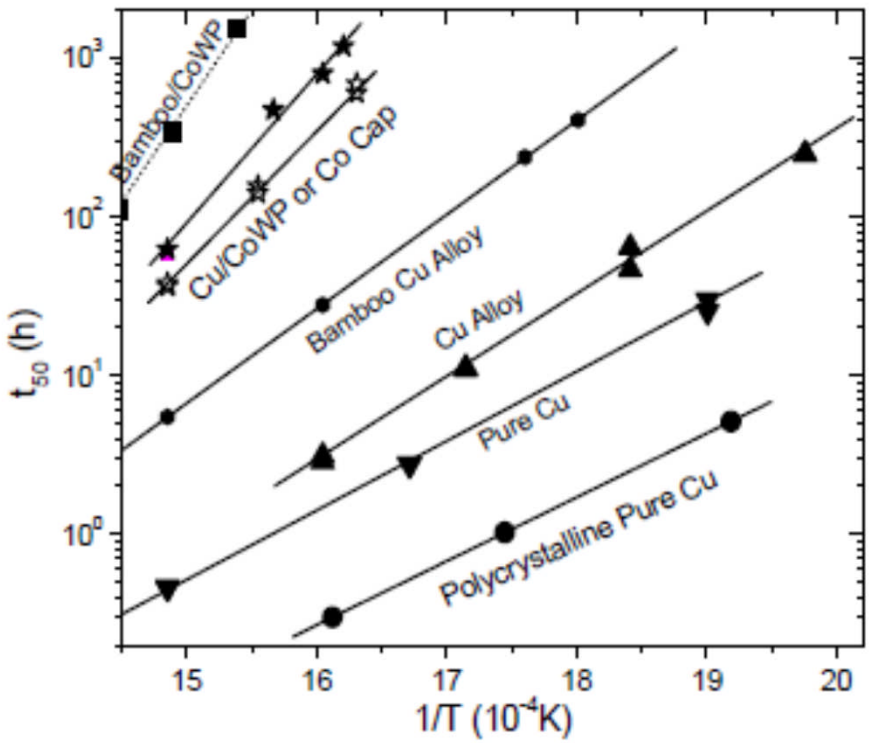
Microstructural effects on metallization lifetime

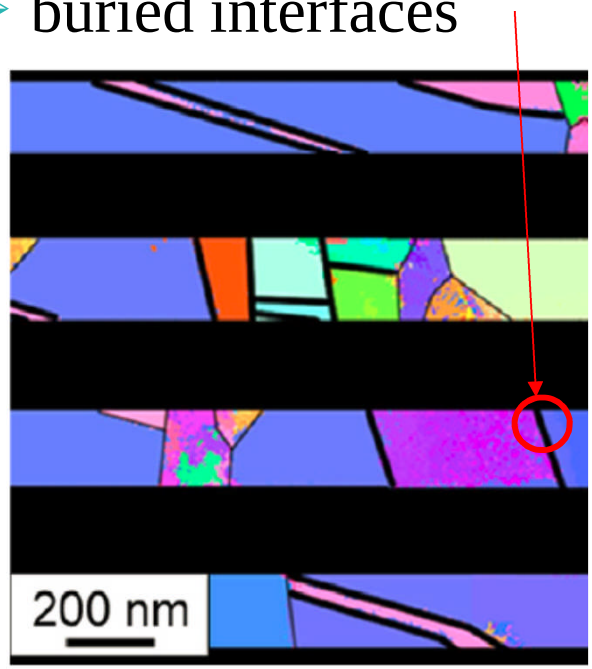


C.K. Hu et al., MRS Symp. Proc. 1559 (2013)

- electrical measurements provide aggregate response over all grains

Follow interfacial dynamics *in-situ* along key interfaces:

- between specific grains
- buried interfaces



K. Ganesh et al., Nanotech. **23**, 135702 (2012)

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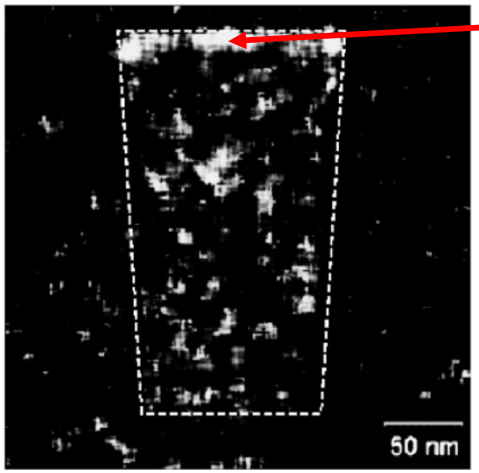
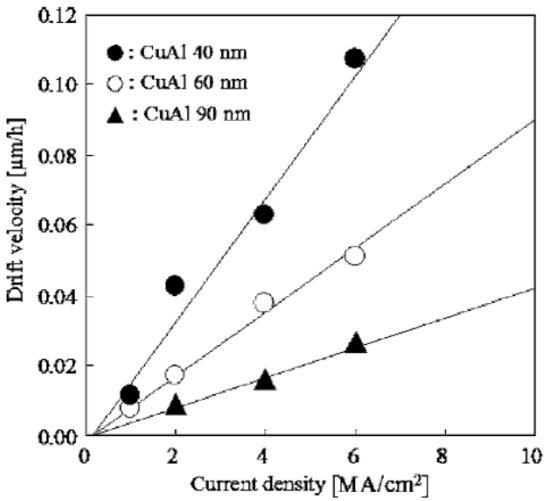
Alloying elements: Cu(Al) metallization

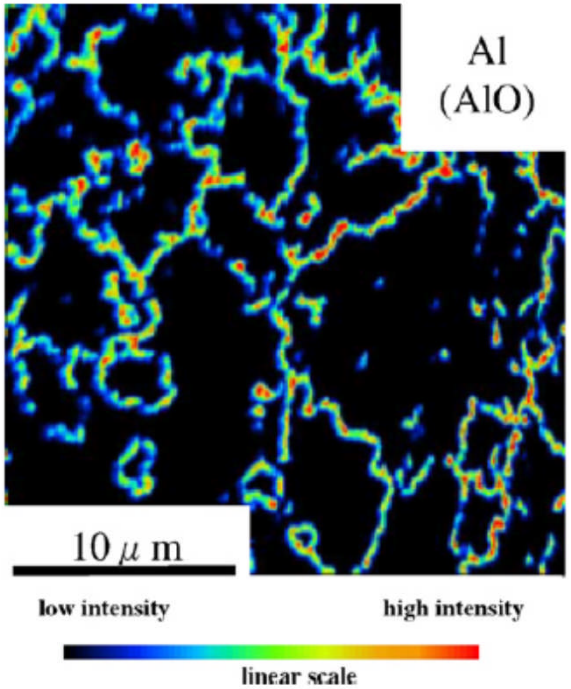
Microprobe analysis





S. Yokogawa et al., JAP **101**, 348 (2007)

- incorporation of Al atoms in Cu seed layer
  - significant diffusion of Al (bottom to top interface)
  - reduction in Cu diffusion scales with dopant quantity



K. Maekawa et al., Micro. Eng. **85**, 2137 (2008)

  - increase in resistance due to impurities
  - segregation to GB's, interfaces

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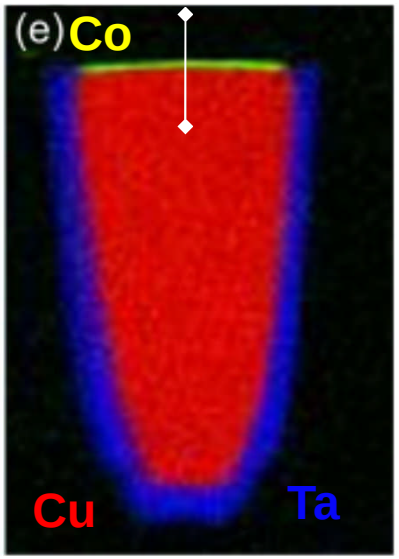
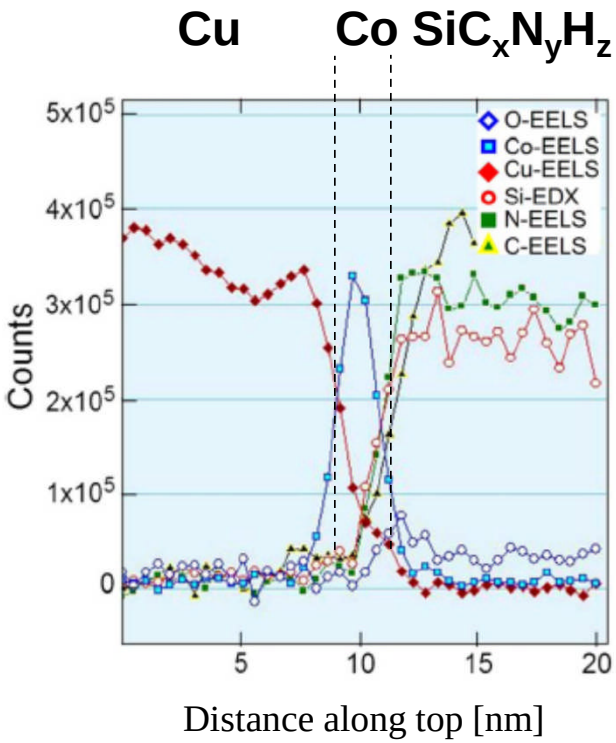
Selective capping



C.C. Yang et al., IEEE EDL 33, 588 (2012)

XTEM characterization



- metallic capping of top surface of metallization
  - mitigate Cu diffusion
  - can we assess bonding state of capping atoms?

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Summary & Conclusions

End of traditional device scaling (lithographic) provides new opportunities

- Silicide-based contact metallization must be more robust
  - placement of impurities with respect to NiSi / Si interface
- Tailoring strain in devices enables more efficient computing
  - *in-situ* determination of three-dimensional strain distributions
- Tunneling mechanisms requires new materials
  - precise location of Hf, O, other elements important to determine V_t
- Metallization needs to survive higher current densities
  - quantification and location of impurities key to mitigate: electromigration, TDDB

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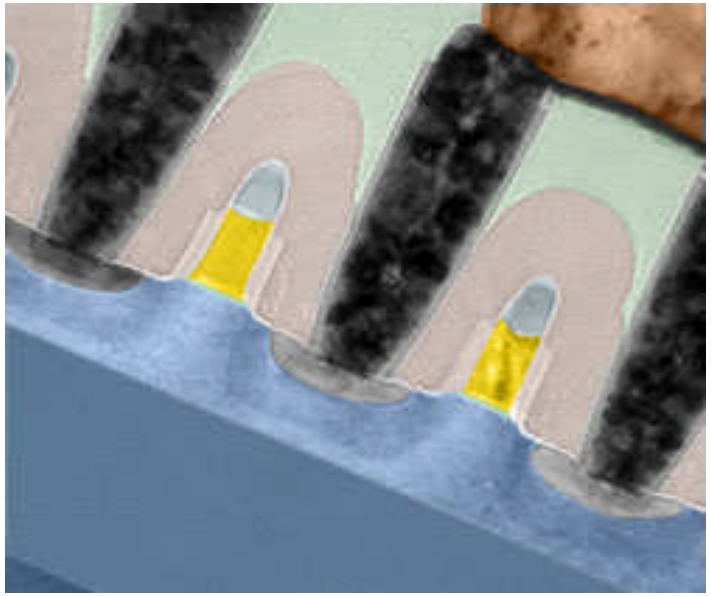
Opportunities of APS Upgrade

- in-situ, spatially-resolved measurements are critical to understanding diffusion-based phenomena in nanoelectronic materials
- combination of complementary techniques
  - diffraction / coherent imaging
  - XANES / EXAFS
  - time-resolved fluorescence tomography
- analyze dopant distributions, chemical state as a function of time, temperature
  - CMOS devices / FinFET's
  - metallization, contacts



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